FREQUENCY SYNTHESIS APPLICATIONS OF SIGE BICMOS PROCESSES

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FREQUENCY SYNTHESIS APPLICATIONS OF SIGE BICMOS PROCESSES

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To my wife, Karla, and my son, Jonathan

two of the best motivations to leave behind the idyllic life of a student.

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SUMMARY

Silicon Germanium BiCMOS technology has been demonstrated as an ideal platform for highly integrated systems requiring both high-performance analog and RF circuits as well as large-scale digital functionality. Frequency synthesizers are ideal candidates for this technology because the mixed-signal nature of modern frequency synthesis designs fundamentally requires both digital and analog signal processing. For applications requiring a high quality frequency source that is also fully integrated on a single die, SiGe offers capabilities not available in any other integrated circuit platform. This research targets three areas to improve SiGe frequency synthesizers. A majority of this work focuses on applying SiGe frequency synthesizers to extreme environment applications such as space, where low temperatures and ionizing radiation are significant design issues to contend with. This includes development of a theory to statistically characterize random radiation-induced transients in microwave oscillators [36], characterization of radiation mitigation techniques in frequency synthesizer charge pumps [42], and budding development of a new measurement technique for capturing bit error impact from transients on mixed-signal frequency synthesizers. A second focus area involves using SiGe HBTs to minimize noise in frequency synthesizer circuits. Improved low frequency "pink" noise in SiGe HBTs provide a significant advantage over CMOS devices, and frequency synthesis circuits are significantly affected by this type of noise. However, improving thermal "white" noise is also considered. These studies include an analysis of phase noise in matched-performance complementary *npn* and *pnp* SiGe HBTs that lead to some interesting inferences to device design [40] as well as efforts to push the residual phase noise floor capabilities of SiGe HBTs in digital frequency dividers [38]. Finally, an

analysis of AM-PM distortion as applied to autonomous circuits such as oscillators will be explored [37]. We expect these new techniques to lead to higher efficiency and lower noise in RF oscillators. Many of the studies presented focus on identifying the physical mechanisms of observed phenomena, such as single event transients or phase noise characteristics in oscillators. The results seek to identify and test design techniques to take advantage of these phenomena, ultimately providing a reference for circuit and system designers seeking to take advantage of the properties of SiGe device physics.

CHAPTER I

INTRODUCTION

Certain technological advances provide such an influence on life and culture that it defines the lens through which we view subsequent history. For example, advances in smelting copper and tin ores lead to the Bronze Age, while the steam engine resulted in the Industrial Revolution. The solid-state transistor is another such technology; creating the backbone of what we commonly refer to as the Information Age. Though only 60 years old, the transistor is the ubiquitous electronic building block that has already transformed our tools and appliances and is rapidly moving into other areas such as our bodies [81]. In that time, the number of transistors in existence has grown exponentially, while the cost and size per transistor has fallen at nearly the same rate [20]. This phenomena has been partially quantified through the well-known Moore's Law, after Intel's Gordon Moore who first observed it during the nascent period of the mid-1960's. Shown in Figure 1, the "law" predicts that the number of transistors, and hence processing power, will double every two years. Due to it's wide acceptance in the semiconductor industry, Moore's Law has been a largely self-fulfilling prophesy since it is used to set research and development targets. Complementary Metal Oxide Semiconductor (CMOS) logic is a natural fit for this paradigm with its maximum logic density and low static power consumption. These are a few of the significant considerations that have made metal oxide semiconductor field effect transistors (MOSFETs) the transistor technology that has driven the Moore's Law curve, and with it the $249 Billion semiconductor industry and many times more in hardware, software, and related services that combine to represent a significant portion of World GDP [55, 82].

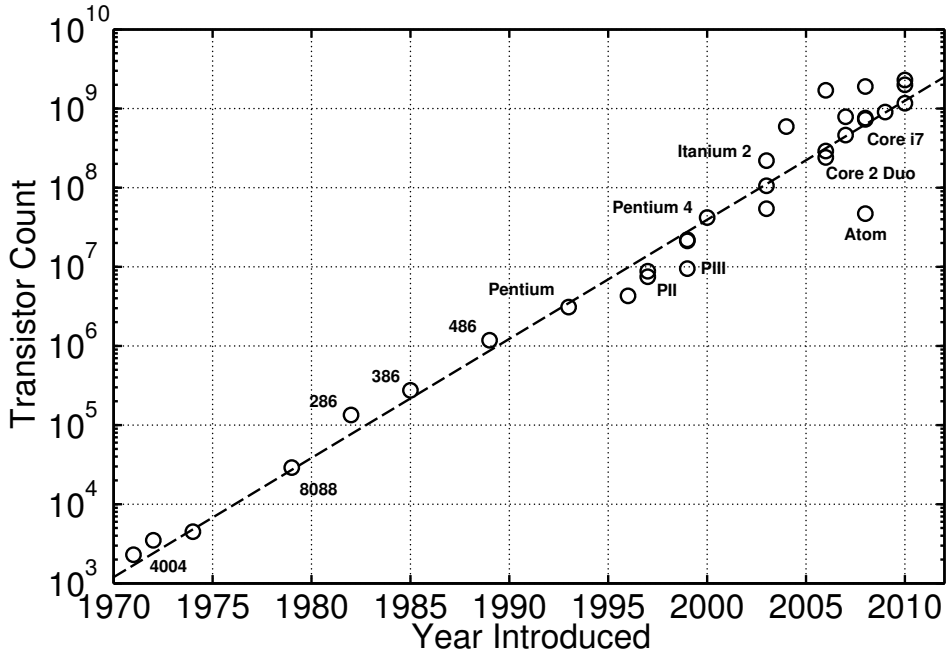
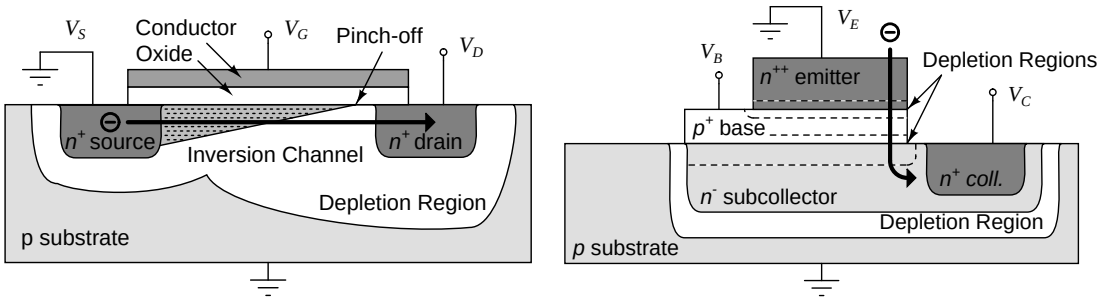


Figure 1: Moore's Law as applied to desktop processors through 2010.

Despite the overall industry domination of CMOS logic, there remain high-performance niche markets where other transistor architectures can still thrive. This is particularly true for the realm of analog electronics. For example, the junction gate field-effect transistor (JFET) is frequently used for its low noise characteristics in high performance audio applications, while the modulation-doped field-effect transistor (MODFET) uses bandgap engineering techniques similar to those discussed in section 1.1 to improve high frequency performance of FET device physics. However, as their names indicate, these devices still rely on the field-effect principle of device operation. For this reason, no device provides a stronger counterpoint to the weaknesses of the MOSFET than the bipolar junction transistor (BJT) and its cousin the heterojunction bipolar transistor (HBT). Invented by William Shockley in 1948, the BJT operates on completely separate solid-state principles from the FET, and actually predates the FET in terms of practical implementation. Despite ceding market dominance to the FET, the BJT still provides ample differentiation to find wide use in



(a) MOSFET (b) BJT

Figure 2: Contrasting field effect and bipolar device physics. An n-channel enhancement-mode MOSFET in saturation is shown in (a), while an npn BJT operating in the forward active mode is shown in (b).

today's analog and RF markets.

At the highest level of abstraction, BJTs and FETs are both three terminal devices that provide gain through transconductance, leading to a first-order similarity in small signal circuit models. Both devices can also be adjusted to operate on electron or hole carriers, producing the capability for utilizing complementary transistors. However, that is where the similarities end. The underlying differences in device physics lead to characteristics that favor certain application-specific spaces for each device.

In general, field effect devices operate by using electric fields to create an inversion layer that produces a channel for charge to pass from one terminal to another [87]. A specific visualization of this procedure is shown in Figure 2a for an n-channel enhancement-mode MOSFET operating in the saturation region. Once the gate voltage, V_G, relative to ground exceeds a certain threshold voltage, V_T, the positive charge deposited on the top plate of the capacitor formed by the oxide will attract enough electrons to the adjacent "plate" of p-type semiconductor to create a channel of negative charge between the n-type source and drain. As the voltage across the drain, V_D, increases relative to ground, a horizontal electric field will form in the channel that accelerates electrons through and produces gain. When V_D has exceeded the overdrive voltage that creates the channel, $V_G - V_T$, the channel pinches-off at the

drain. Electrons are then pushed through the depletion region by the strong electric field at a constant rate defined by the saturated drift velocity of the carrier. Ignoring other second-order effects, the current flowing through the drain in this region of operation is known as the square-law relationship and can be defined as

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_G - V_T)^2, \tag{1}$$

where W and L represent the lateral width and length of the channel respectively. The first term encompasses electron carrier mobility, μ_n, and oxide capacitance, C_{ox}, which will be technology-dependent factors. Technology nodes in MOSFETs are defined by the minimum channel length, L, capable of being fabricated, which will be directly proportional to the speed of the device. The square-law relation holds for a MOSFET in strong inversion and strong saturation, which becomes more difficult to achieve in technology nodes below 1 μm.

In contrast, the *npn* bipolar device is shown in Figure 2b. As the base voltage, V_B, relative to ground increases beyond the thermal voltage, the diode formed between the base and emitter begins conducting. The thermal voltage is given as

$$U_T = \frac{kT}{q}, \tag{2}$$

where k is the Boltzmann constant, T is the absolute temperature, and q is the magnitude of charge on an electron. Because the emitter is doped several orders of magnitude greater than the base, the resulting charge flow will be dominated by electrons from the emitter, with very few holes being contributed by the base. If the collector voltage, V_C, is greater than V_B, the junction between collector and base is reverse-biased, and will have a reverse bias leakage current proportional to the number of minority electron carriers in the base that come within a diffusion length of the junction. If the base is sufficiently narrow, the base-emitter junction can be thought of as minority carrier injector into the base. However, rather than flowing

out of the base node as would be the case of a typical diode, the minority carrier electrons are swept to the collector through drift because of the large electric field created by the reverse-biased base-collector junction [87]. The carrier disparity in the base-emitter junction creates current gain by having a small base current contribution control a significantly larger emitter current. In the forward active mode described, the exponential relationship describing carrier generation in the base-emitter junction and the linear relationship governing hole diffusion in the base-collector junction combine to form the Ebers-Moll transfer characteristic given as

$$I_C = \alpha_T I_{ES}(\exp^{V_B/U_T} - 1), \tag{3}$$

where I_{ES} is the reverse saturation current of the base-emitter junction and α_T is the efficiency of the transfer from emitter current to collector current.

The preceding comparison exercise reveals a number of critical differences in FET and BJT device operation. Observing the forward transfer characteristics from input voltage to output current in (1) shows a quadratic nonlinearity for the FET and in (3) shows an exponential nonlinearity for the BJT. The exponential relationship increases much faster than the quadratic for a similar input voltage. Therefore the transconductance, g_m, which is defined as the slope of this characteristic, will be inherently higher for the BJT. Transconductance is a critical parameter in defining the gain of an analog circuit design, and implies that the BJT can achieve larger gains at smaller drive levels.

Another important distinction is that the FET is a unipolar majority carrier device, while the BJT is a bipolar minority carrier device. This can be illustrated by imagining an electron test charge at the emitter of the BJT or source of the FET, denoted by $\ominus$ in Figure 2. In the MOSFET, the electric field from drain to source pulls the electron from source, to channel, to drain entirely through n-type material (and briefly through the pinched-off depletion region) when operating in

saturation mode. Because all regions are the same type, the minority hole carriers will not make a significant contribution to the current, making the device operate in a unipolar fashion on majority carriers only. In contrast, the forward-biased base-emitter junction of the BJT injects the electron from the emitter into the p-type base where it is a minority carrier. This transport is a diffusion-dominant process that will also involve some flow of holes for base recombination as well as a small contribution of the total forward-bias current flow. The electron carrier in the base is then swept across the reverse-biased base-collector junction through drift as described previously.

Note from the direction the test charge travels in Figure 2 that the MOSFET is a horizontal transport device while the BJT is a vertical transport device. This is important because the speed of a device is limited by the time it takes a carrier to traverse from one terminal to another. This is the reason that speed in a MOSFET is determined by the channel length, a horizontal dimension. During fabrication, minimum channel length will be tied to the limits of photolithography. Reducing this dimension has been key to maintaining the Moore's Law curve in Figure 1, but concerns over device reliability are causing many to question the physical limits of lithography scaling [46, 47]. On the other hand, the vertical nature of the BJT means that reducing the vertical dimension of the base between the emitter and subcollector, commonly referred to as the base width, will increase speed. During fabrication, base width is determined primarily by the thermal cycles after ion implantation. Because the focus on reducing base width has been less intense over the past forty years, there is less concern that fabrication techniques to minimize this dimension are approaching fundamental physical limits. Thus, the present technology landscape implies that there is more growth potential for high speed devices in BJT-style technology. Also, the massive costs involved in fabricating the smallest lithography nodes make large volumes necessary in order to be economically viable. Thus, lower volume analog and RF products often make the BJT a more cost effective high speed solution.

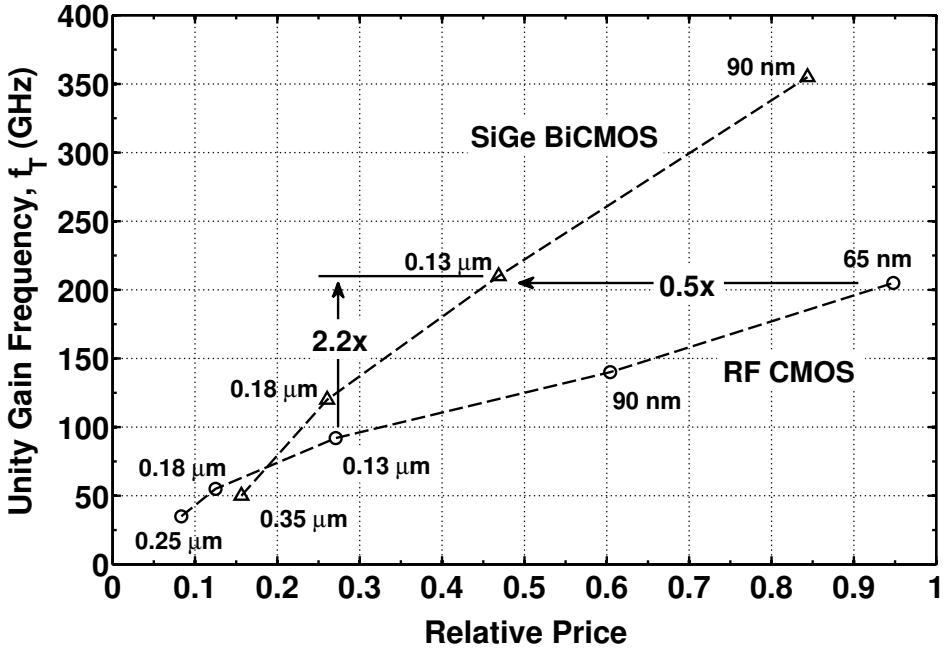


Figure 3: Device speed as a function of relative price for various lithography nodes of RF CMOS and SiGe BiCMOS technologies [45]. SiGe BiCMOS offers twice the unity current gain frequency, f_T, at comparable lithography nodes, or half the price at comparable f_T.

Low power applications tend to favor the FET for a number of reasons. First, the capacitive coupling of the FET gate voltage implies no current draw for a first order DC calculation, compared to the BJT, which from first principles will always require some base current. This is best expressed by saying that the FET has a higher input impedance than the BJT. Another reason the FET is better for low power operation, the onset of the inversion channel is set by the threshold voltage, V_T. This value can be tailored by a number of process-dependent variables such as oxide thickness, doping levels, surface charge, etc. Hence, V_T can be engineered to the desired level for a given process. However, in order for emitter carrier injection to occur in the BJT, the base-emitter junction must overcome its built-in potential, a value that will always be near 0.7 V based on the necessary doping levels. Having this ability to operate at lower voltages means the FET will draw less power, but it comes at the expense of device matching. The myriad of process-dependent parameters that determine V_T will entail greater variation across wafer lots and between devices on the same circuit relative to the BJT.

An exhaustive list of differences could continue, but the emerging trend would be the same. MOSFETs are generally better suited to low power, high density applications where the device can behave as a switch, such as digital circuitry. BJTs provide performance advantages in high speed analog and RF applications where the device operates in between fully on and fully off conditions. These contrasts will eventually provide a guide to exploring frequency synthesis applications where both BJT and FET device physics are desired in the same circuit.

1.1 Introduction to the SiGe HBT

The heterojunction bipolar transistor (HBT) is an extension of the device physics underlying the BJT. These devices modulate the bandgap of the BJT as carriers traverse the base to enhance desired performance aspects, a process known as bandgap

engineering. In semiconductor materials, the bandgap can be adjusted by introducing an alloy of another material into a single crystalline growth. This technique is used to produce the highest performance transistors available using a number of different materials including: Gallium Arsenide (GaAs), Indium Phosphide (InP), and Gallium Nitride (GaN). However, there is currently only one physically realizable Silicon-based heterostructure that combines the performance of bangap engineering with the processing advantages of Silicon: the Silicon Germanium (SiGe) HBT.

Development of the SiGe HBT has spanned many decades. Although the original concept was first considered by William Shockley during development of bipolar device physics, it took over thirty years to produce a working prototype due to limitations in fabrication capability. An excellent history of SiGe process development is given in [18]. When Germanium atoms are substituted for Silicon atoms in the diamond lattice crystalline structure, a narrowing of the bandgap occurs primarily through the valence band that is a function of the amount of Germanium in the alloy [74]. By precisely controlling the Germanium content during a chemical vapor deposition growth, a Germanium profile spanning the width of the base results in controlled modulation of the device bandgap. The limits of this effect are determined by the stability of the crystal alloy. Silicon and Germanium have different lattice constants, resulting in a lattice mismatch of 4.1%. Therefore, creating a single-crystalline SiGe alloy produces strain on the crystal, which will produce defects when the Germanium content exceeds a stable limit of thickness.

There are multiple effects that can be achieved by altering the bandgap of a bipolar transistor. Consider a linearly ramped Germanium profile and corresponding band diagram highlighted by Figure 4. The start of the neutral base region is set as the origin, $x = 0$, while the other end of the neutral base is at $x = W_b$. The bandgap is the difference between the conduction and valence bands, and is shown for both the Si BJT and SiGe HBT in the band diagram of Figure 4. The bandgap narrows

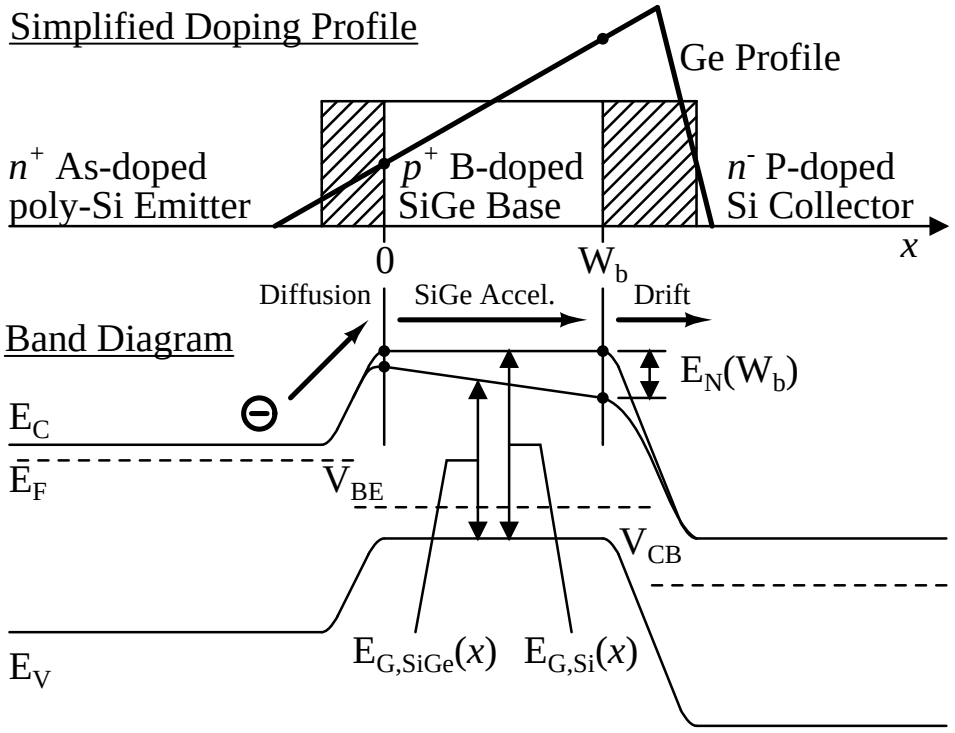


Figure 4: A ramp Germanium profile creates an electric field that accelerates minority carriers through the neutral base, improving base transit time and output impedance.

as the Germanium content increases across the width of the neutral base, producing the sloped conduction band seen in the SiGe band diagram. In this case, the valence band slope induced by the Germanium transfers to the conduction band because the Fermi-level of the p-type base is tied to the valence band and must be flat under equilibrium conditions [21].

Band diagram fundamentals reveal that the introduction of the sloped neutral base region corresponds to an electric field that will push minority carriers through the neutral base according to traditional drift carrier transport. This field has two important effects on static device characteristics. First, it will reduce the base transit time of minority carriers, improving the speed of the device. Let the position-dependent bandgap narrowing of the SiGe HBT relative to the Si BJT be given by E_N, such that

$$E_N(x) = E_{G,Si}(x) - E_{G,SiGe}(x). \tag{4}$$

For the case of the linearly ramped Germanium profile, the grade of the bandgap across the neutral base can be given as

$$\Delta E_N = E_N(W_b) - E_N(0). \tag{5}$$

Using this notation, derivations for the improvement of SiGe HBTs relative to a comparable Si BJT have been given in [21]. For the base transit time, the result is

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\eta}\frac{kT}{\Delta E_N}\left[1 - \frac{kT}{\Delta E_N}\left(1 - e^{-\Delta E_N/kT}\right)\right], \tag{6}$$

where η is the ratio of averaged diffusivity parameters between Si and SiGe. For steep Germanium grading ($\Delta E_N \gg kT$), the result reduces to

$$\left.\frac{\tau_{b,SiGe}}{\tau_{b,Si}}\right|_{\Delta E_N \gg kT} \approx \frac{2}{\eta}\frac{kT}{\Delta E_N}. \tag{7}$$

This approximation reveals that the base transit time reduces proportional to the energy grade, and hence, the magnitude of the electric field, which makes intuitive sense. Likewise, a shallow Germanium grade ($\Delta E_N \ll kT$) can be shown to reduce to nearly unity by expanding the exponential term in a Taylor series. This result shows that a constant bandgap narrowing will produce no transit time enhancement. Instead, the electric field created by grading the profile is essential to achieving this effect.

The introduction of a graded Germanium profile will also increase the output resistance of the HBT by impeding changes in the depletion region of the base-collector junction through the generalized Moll-Ross relation [21]. This effect is manifest in the Early voltage metric used to characterize output resistance. The improvement in Early voltage for the SiGe HBT relative to the Si BJT has been derived as

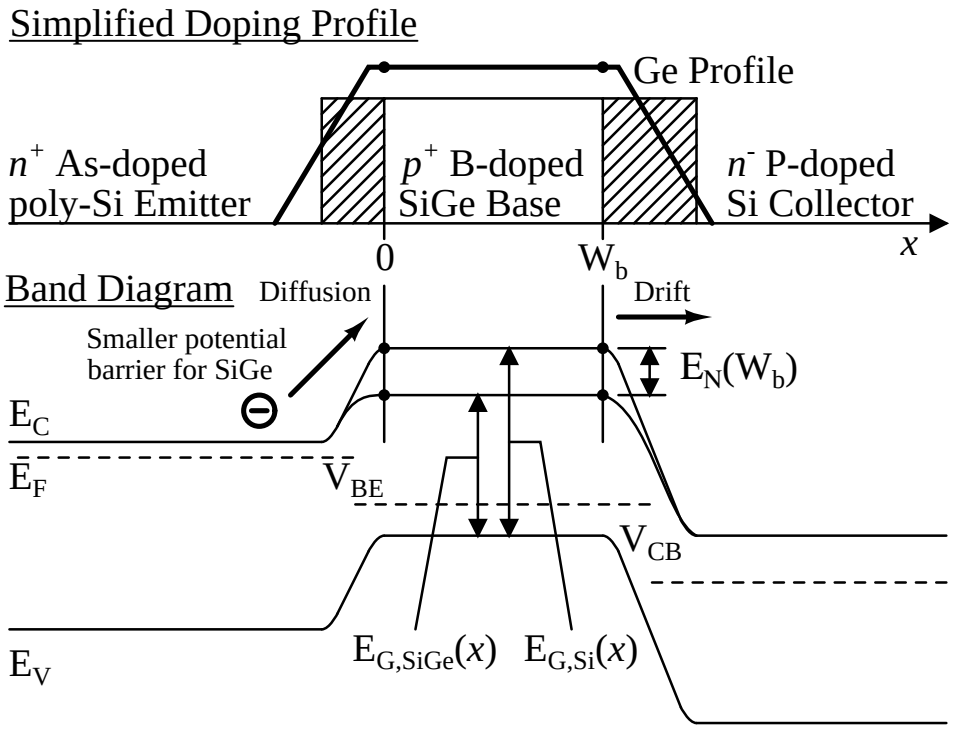


Figure 5: A profile with large Germanium content at $x = 0$ reduces the potential barrier for minority carrier injection into the base, improving DC current gain and small signal transconductance for a fixed bias voltage.

$$\frac{V_{A,SiGe}}{V_{A,Si}} \approx e^{\Delta E_N/kT}\left(\frac{1-e^{-\Delta E_N/kT}}{\Delta E_N/kT}\right). \tag{8}$$

Again, there is a strong dependence on the grade of the Germanium profile, with a steep grade reducing (8) to

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{\Delta E_N \gg kT} \approx \frac{e^{\Delta E_N/kT}}{\Delta E_N/kT}, \tag{9}$$

and a shallow Germanium grade reducing to unity, indicating no change between the SiGe HBT and a similar Si BJT.

Contrast the graded Germanium profile of Figure 4 with the box profile shown in Figure 5. Here, the added Germanium uniformly reduces the bandgap across the neutral base. Since there is no electric field induced by the sloping bandgap, the transit time improvements are not present here. Instead, the bandgap narrowing has

reduced the potential barrier at $x = 0$ in the emitter-base junction, allowing many more minority carriers to diffuse from the emitter into the base at a fixed bias voltage. This effect increases the DC current gain since there is not a significant increase in base recombination, meaning the base current remains nearly identical to the Si BJT. The current gain enhancement has been derived as

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \gamma\eta\frac{\Delta E_N}{kT}\frac{e^{E_N(0)/kT}}{1 - e^{-\Delta E_N/kT}}, \tag{10}$$

where γ is the effective density of states ratio between SiGe and Si; a value that will be less than 1. Note that Germanium grading will also play a role in determining the DC current gain, but the exponential term in the numerator of (10) will dominate the enhancement. For the box profile of Figure 5, the bandgap grade across the neutral base is negligible, allowing (10) to reduce to

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{\Delta E_N \ll kT} \approx \gamma\eta e^{E_N(0)/kT}. \tag{11}$$

A hybrid of the box and linear ramp profiles can also be used. These are referred to as trapezoidal profiles and often feature significant Germanium content at $x = 0$ as well as a linear ramp across the neutral base. Assuming the average Germanium content remains the same to preserve the stability of the strained SiGe, the current gain enhancement for a steep Germanium grade can be approximated as

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{\Delta E_N \gg kT} \approx \gamma\eta\frac{\Delta E_N}{kT}e^{E_N(0)/kT}. \tag{12}$$

The addition of Germanium enhances a number of parameters relevant to circuit design. In addition to the design metrics provided above, the βV_A product is an often used figure of merit for bipolar analog design. To arrive at this product for a SiGe HBT, a simple combination of (10) and (8) gives

$$\frac{\beta V_{A,SiGe}}{\beta V_{A,Si}} = \gamma\eta e^{E_N(0)/kT} e^{\Delta E_N/kT}. \tag{13}$$

Note that this product combines two exponential functions to provide a significant improvement over the Si BJT no matter what Germanium profile is used. Another important feature that falls from this analysis is that each equation defining the effects of bandgap engineering in the SiGe HBT is relative to the thermal voltage, kT. Thus, as temperature decreases the circuit parameters increase proportionally. Leveraging this technique has produced record speeds in silicon-based circuits [48].

With a wide number of profile combinations and a scarce amount of Germanium available due to stability limits, Germanium profile design is an application-dependent engineering problem with numerous trade-offs to consider. It is little wonder then that the profiles for commercial foundries are highly sensitive intellectual property. However, a snapshot of several state-of-the art SiGe processes from 2006 can be found in [18]. The role of the circuit designer is to have a basic understanding the primary device physics outlined here as well as the second order effects that also impact circuit parameters. The focus now turns to understanding the system requirements that govern modern communication systems in order to find intersection points that can be used to improve performance and efficiency.

1.2 Introduction to Frequency Synthesis

Wireless communication systems transmit and receive information using a link consisting of the physical free space surrounding the transceivers. Unlike wired communication systems whose link between transmitter and receiver is restricted to the confines of a shielded cable, all wireless systems must share the same communications channel. This makes the transmission of raw information a practical impossibility unless everyone agreed that only one wireless device would operate in a given physical proximity. Consider the analog transmission of audio information. The compression

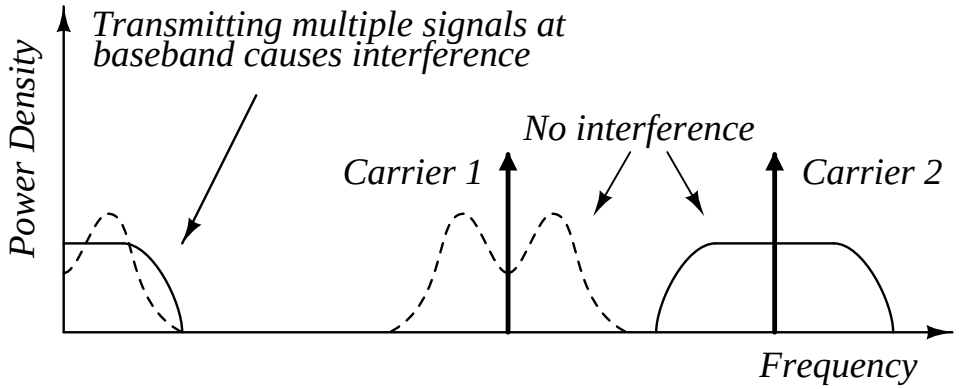


Figure 6: Motivation for using carrier modulation to transmit wireless signals.

waves that make up the sound are converted to electrical signals with spectral components limited from 10 Hz to 5 kHz. If two different signals were transmitted in this raw form over the same wireless space, the receiver would capture a superposition of both signals with no way to extract the original signal from either transmitter without knowing their contents ahead of time.

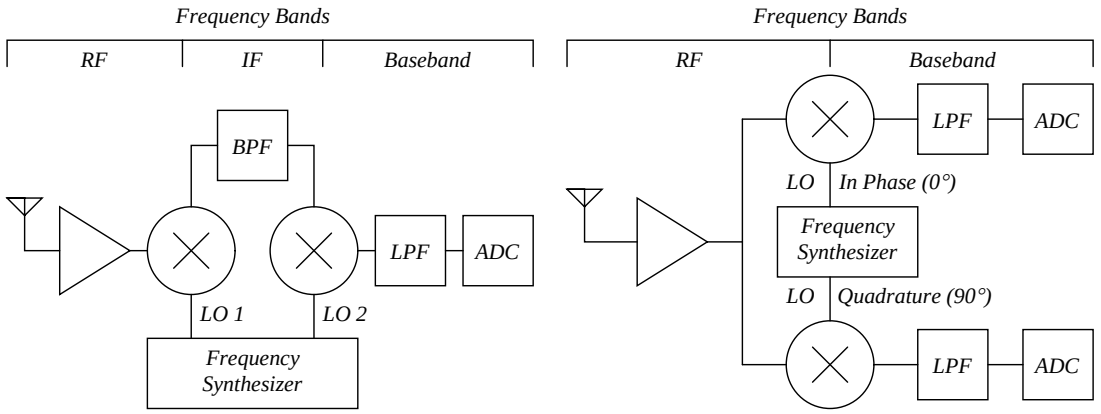
Wireless transceivers overcome this problem by modulating the raw information onto a high frequency "carrier". Using a spectrally pure sinusoid, system designers can choose to modulate the amplitude or phase of the carrier signal [27]. Phase modulation encompasses several techniques including modulation of the frequency, which is the time-derivative of phase, and directly modulating the phase offset. By utilizing orthogonality properties of these sinusoids, multiple modulations can occupy the same spectrum, increasing the amount of information transmitted over a fixed time period. Continuing with the previous example of analog audio information, let one signal be amplitude modulated (AM) onto a carrier frequency of 890 kHz, while the other is on a carrier of 930 kHz. These two signals can now be transmitted and received simultaneously without interference as shown in Figure 6. This is the essence of AM radio transceiver operation, but applies to all wireless transmission schemes.

For the reasons described, all wireless transmissions rely on the generation of

a carrier signal. Even if the carrier is suppressed during transmission to improve transmission efficiency, the carrier must be recovered by the receiver in order to demodulate the information. In order to preserve the integrity of the information being transmitted as well as the strict frequency band requirements, the carrier signal should be as close to a pure sinusoid as possible. Added noise, harmonic distortion, and frequency instability in the carrier will degrade the performance of the entire transceiver. Design factors such as efficiency, size, and cost are also a consideration. These requirements are typically met through the use of a frequency synthesizer. Synthesizers in modern communications systems are mixed-signal systems composed of analog, RF, and digital circuit blocks designed to produce stable and pure frequency sources.

Frequency synthesizers also play a critical role in channel selection. Most communications systems employ several channels that a receiver must select between. Channel selection is typically made by tuning the frequency synthesizer to multiple precise frequencies. In some applications, agile frequency synthesis requires a synthesizer that can switch between stable frequencies within a specified time. The focus of this work is to apply the advantages of the Silicon-Germanium heterostructure described in Section 1.1 to improve the performance of this critical block for wireless communications.

There are many types of transceiver architectures that demand different performance specifications from a frequency synthesizer. Figure 7 shows two popular schemes with contrasting requirements. The heterodyne architecture is shown in Figure 7a, featuring conversion from the RF transmission frequency to an intermediate frequency (IF) before a final downconversion to baseband. This technique has been a staple of wireless systems dating back to the earliest implementations. The IF frequency provides relief for stringent filtering requirements needed to select between multiple channels of information. Frequency synthesizers for this application need



(a) Heterodyne Receiver (b) Quadrature Homodyne Receiver

Figure 7: Two popular receiver architectures with different frequency synthesizer requirements. (a) represents a heterodyne receiver requiring generation of two frequency tones, while (b) shows a homodyne architecture with quadrature downconversion requiring both in-phase and quadrature signals at the same frequency.

to generate two frequency tones to accommodate the extra frequency band. Phase of the signals are not important in this implementation because there is no quadrature requirement. This contrasts with the homodyne receiver in Figure 7b. Here, the transmitted RF signal is converted directly to baseband. This requires only one carrier frequency for translation, but the quadrature requirement means the phase between two carrier signals must be well-controlled to 90 degrees. Quadrature is a technique that takes advantage of the orthogonality between sine and cosine functions to transmit two signals on the same carrier frequency [76]. Typically, these signals are the real and imaginary parts of a complex waveform, leading to the transmission of coherent data that can be used for applications ranging from high data rate digital communications to radar.

1.2.1 Oscillator Basics

The fundamental circuit that powers the frequency synthesizer is the electronic oscillator. This is an autonomous circuit that requires no forced input to operate. Instead, it uses positive feedback to build small circuit noise into strong oscillating

waveforms at a desired frequency. The loop gain of the oscillator is limited by the non-linearities of the active device until an equilibrium is reached that produces a stable limit cycle. There are many types of electronic oscillators, including ring oscillators, multi-vibrators, and resonant tank oscillators. Frequency synthesis for wireless communications requires low noise, sinusoidal waveforms with little harmonic content, and high frequency operation. Oscillators that depend on a circuit resonance are generally preferred for this application.

There are multiple ways to visualize the operation of a resonant tank oscillator. One way is to consider the oscillator as a the combination of a gain stage and a frequency selective stage as shown in Figure 8a. The summed term, v_e, combines the noise of the circuit, v_n, with the positive feedback term to give

$$v_e = v_n + A\beta v_e. \tag{14}$$

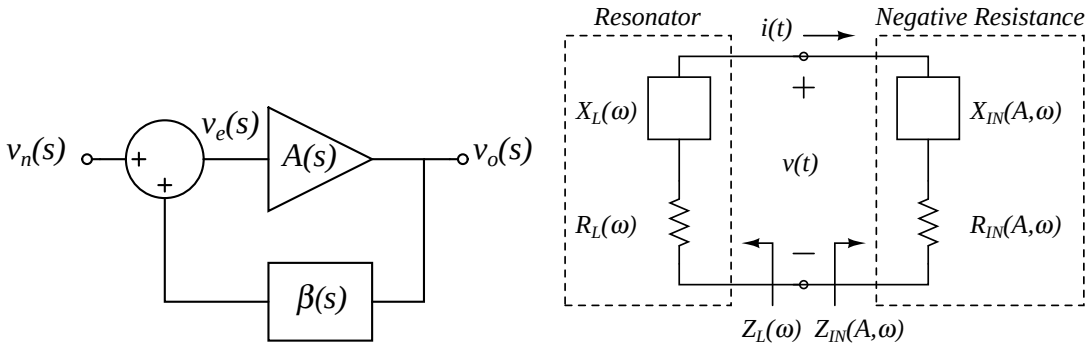
The output of the oscillator can be given as

$$v_o = Av_e, \tag{15}$$

leading to a closed loop transfer function from input noise voltage to output voltage of

$$\frac{v_o}{v_n} = \frac{A}{1 - A\beta}. \tag{16}$$

Since A and β are both complex variables, the relationship in (16) leads to the familiar Nyquist criteria for oscillation [30]. When $|A(s)\beta(s)| > 1$, the poles of the system will be in the right-half of the s-plane, resulting in a growing oscillation. This is the requirement necessary to start self-sustaining oscillations, with the magnitude of the $A\beta$ product known as the loop gain. In practical applications, nonlinearities will reduce the loop gain as v_e increases, creating a stable oscillation at the point where



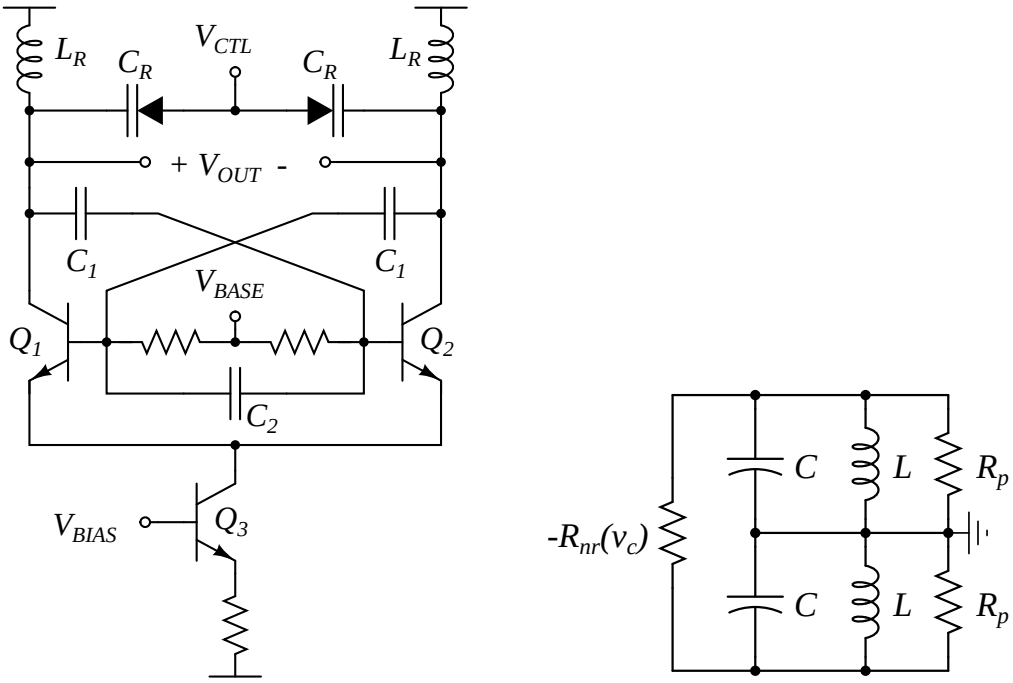
(a) Positive Feedback Model (b) Negative Resistance Model

Figure 8: Two equivalent methods for deriving oscillation conditions.

the loop gain equals 1. The second condition for oscillation is that $\angle A\beta = 2n\pi$, where n is an integer. This condition ensures that the input and feedback signals are in phase and therefore add constructively to produce a growing oscillation. Since $\beta(s)$ is a frequency selective function, this condition should only be met at a single frequency, thus setting the frequency of oscillation.

An alternative technique for considering the design of microwave oscillators is the negative resistance method [30]. This design procedure produces equivalent results to the feedback analysis presented previously, but is preferred in situations where device parasitics or distributed passive elements make feedback analysis difficult. A general formulation for the analysis is shown in Figure 8b. The circuit consists of a passive frequency-dependent element shunted with an active element that is dependent on both the frequency and the magnitude of the standing wave on the interface node.

A simple LC resonant tank illustrates the negative resistance concept. A combination of lumped inductor, L, and capacitor, C, in series will produce the reactive impedance $X_L(\omega)$ in Figure 8b with resonant frequency ω_0. Practical components will always have some loss associated with them, which is lumped into the resistive term R_L. The negative resistance is made up of active devices either by themselves or in configurations such as the cross-coupled pair. Consider a negative resistance that introduces little reactive impedance or frequency dependence so that it can be



(a) Circuit Schematic (b) Behavioral Description

Figure 9: A behavioral analysis of the cross-coupled negative resistance oscillator including (a) the original circuit schematic and (b) the behavioral simplification used to gain insight into the control mechanics of the system.

modeled entirely by $R_{IN}(A)$. The series resonance of the tank can be expressed as an equivalent parallel circuit, placing the equivalent loss of the resonator, $R_{L,P}$ in parallel with the negative resistance $R_{IN}(A)$. As long as $|R_{IN}(A)| > R_{L,P}$, the circuit will be unstable and oscillations will grow. As the amplitude, A, of these oscillations increase, $R_{IN}(A)$ will reduce until $R_{IN}(A) = R_{L,P}$ producing a steady-state oscillation. Formal derivations of this concept are given in [30] to show that the conditions for stable oscillation are given as:

$$R_L(\omega_0) + R_{IN}(A_0, \omega_0) + j[X_L(\omega_0) + X_{IN}(A_0, \omega_0)] = 0 \tag{17}$$

$$\left.\frac{\partial R_{IN}(A)}{\partial A}\right|_{A=A_0} \left.\frac{\partial X_L(\omega)}{\partial \omega}\right|_{\omega=\omega_0} - \left.\frac{\partial X_{IN}(A)}{\partial A}\right|_{A=A_0} \left.\frac{\partial R_L(\omega)}{\partial \omega}\right|_{\omega=\omega_0} > 0 \tag{18}$$

A behavioral model of the oscillator feedback mechanism is useful for gaining insight, and will be used here during analysis of the fundamentals of ion-induced

transients in a space environment. A common implementation of the negative resistance oscillator is shown in Figure 9. This circuit generates the negative resistance, R_{IN}, across the collector nodes of the cross-coupled transistors, Q_1 and Q_2, with the RC combination on the base and the tail current present for biasing purposes. This design is ubiquitous in integrated circuit implementations for its good noise performance and ease of design. The circuit schematic of Figure 9a is reduced to an equivalent behavioral model shown in Figure 9. The output is observed as the voltage across the capacitor, $v_c(t)$, which has the general form

$$v_c(t) = A(t)\cos(\omega_0 t + \phi(t)). \tag{19}$$

The second-order differential equation that describes the time-domain solution to this model can be classified as a Liénard system, and is expressed as

$$\ddot{v}_c(t) + \frac{1}{C_T \cdot (R_{L,P}\| - R_{IN}(A))}\dot{v}_c(t) + \frac{1}{L_R C_T}v_c(t) = 0, \tag{20}$$

The unforced state of this system is defined entirely by the initial conditions of the voltage across the capacitor, $v_c(0)$, and its first derivative, $\dot{v}_c(0)$, for a given reference time $t = 0$. An alternate derivation using the current through the inductor is equally valid.

Under small-signal conditions, the negative resistance of this stage has been demonstrated as approximately equal to $-2/g_m$, where g_m is the transconductance of one HBT in the cross-coupled pair [77]. In order to capture the nonlinear behavior, we replace g_m with its large signal equivalent, $G_M(A)$, to get

$$-R_{IN}(A) = -\frac{2}{G_M(A)}. \tag{21}$$

By making this substitution, we are assuming that the SiGe HBTs operate in the forward-active mode. Substituting into (20), an equation for the cross-coupled oscillator topology can be given as

$$\ddot{v}_c(t) + \frac{2 - R_{L,P}G_M(A)}{2R_{L,P}C_T}\dot{v}_c(t) + \frac{1}{L_R C_T}v_c(t) = 0. \tag{22}$$

If the cross-coupled transistors are thought of as a differential pair, the large-signal transfer characteristic takes the form of a hyperbolic tangent. A Fourier series expansion reveals that this function is odd and contains no power in even-numbered harmonics. Following the derivation outlined in [13], an expression for G_M can be found to be

$$G_M(A) = \frac{2g_m}{k\pi A}\int_{-\pi}^{\pi} \tanh\left(\frac{kA}{2}\cos\theta\right)\cos\theta d\theta, \tag{23}$$

where k is a scaling factor including the thermal voltage, V_T, defined by

$$k = \frac{C_1}{(C_1 + 0.5C_2)V_T}. \tag{24}$$

No closed-form solution exists for (23). Furthermore, any nonlinearity characteristic applied to (22) prevents closed-form analysis of transient conditions. It therefore becomes necessary to turn to numerical methods and phase-plane analysis to gather insight into single event transients [88]. MATLAB was used to find numerical solutions to (23) across v_c, and Spectre was used to find the solutions to the differential equations using the behavioral model of Figure 9. The nonlinear resistance, R_{IN}, was modeled by importing the numerical solution to (23) via text file to a piece-wise linear voltage-controlled current source. This method of simulation captures the essence of the cross-coupled oscillator without any additional parasitic effects, and will be helpful for understanding the fundamental impact of transients on the general circuit.

1.2.2 Closed Loop Performance

While oscillators are the fundamental building block behind frequency synthesis, a free-running oscillator such as one described in Section 1.2.1 is rarely sufficient to

generate a signal adequate for use in wireless communications systems. Several issues lead to this conclusion. Foremost is the frequency stability of a free-running oscillator at RF frequencies. The relationships that determine the oscillation frequency such as (16) and (17) are subject to noise disturbances. This noise perturbs the oscillation from it's steady state condition proportional to its fractional bandwidth. Therefore, as the frequency of oscillation increases, so does the impact of noise on both frequency stability and phase noise. Frequency instability makes the carrier frequency "bounce" randomly with a Gaussian distribution. At the RF carrier frequencies used in wireless systems, this random fluctuation can significantly increase channel spacing requirements to avoid interference, resulting in inefficient use of scarce spectrum. The effect of phase noise close to the carrier frequency produces similar results, creating a need to reduce the close-in phase noise of the synthesizer. Finally, adjusting the frequency of a free-running oscillator is an analog process with a nonlinear transfer characteristic, making it difficult to precisely control the output frequency of the synthesizer with adequate certainty.

The solution to each of these problems is phase locking. In this process, the output phase and frequency of an RF oscillator is compared to a lower frequency reference source. The lower frequency reference is typically a fixed frequency, high quality crystal that produces extremely stable and low noise sinusoids that exceed the limits of the RF oscillator. Comparisons of phase and frequency between these two sources yields an error term that gives the instantaneous deviation of the RF oscillator relative to this reference. This error term is used to adjust the frequency of the RF oscillator via a voltage control line, creating a servo feedback system. Phase locking has a long history dating back to the beginnings of the electronics industry. Excellent narrative and technical histories of the evolution of this critical subsystem are found in [24, 56].

A variety of techniques have been used to achieve phase locking dependent upon

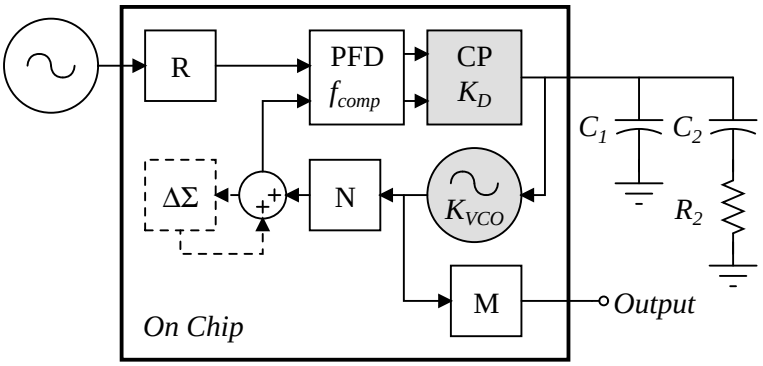


Figure 10: The integer-N and fractional-N frequency synthesizer architectures typically used for integrated circuits.

the application and platform used. On an integrated circuit platform for frequency synthesis applications, two closely-related architectures have dominated based on their small area and power requirements. These mixed-signal solutions are shown in Figure 10. The integer-N architecture consists of all of the solid outlined blocks. This architecture divides the RF oscillator signal by an integer number for comparison with the reference. This solution offers the simplest approach and is suitable for many systems, but often has higher noise for the following reasons. The frequency spacing of the synthesizer is determined by the required channel spacing. Because the divider can only produce integer divisors, the comparison frequency, f_{comp}, must be chosen as the greatest common divisor of the channel spacing and reference frequency. This produces large division values of N, which proportionally increases the in-band noise of the PLL [29].

Fractional-N synthesis adds the accumulator with delta-sigma perturbations shown in the dashed outline of Figure 10. Introducing an additional count after accumulating a given number of output pulses from the divider produces averaged divide ratios that are a fraction of the comparison frequency. For example, consider a feedback divider that reduces the VCO frequency by a factor of three as shown in Figure 11. After accumulating four pulses, the divider is triggered to divide by four to produce

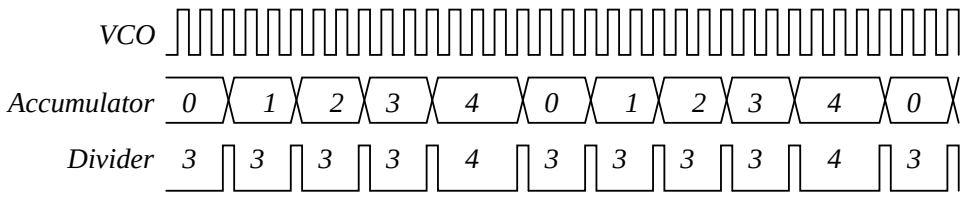


Figure 11: An illustration of fractional-N operation using a simple accumulator. The VCO waveform is shown as a square-wave for simplicity.

the fifth pulse before resetting. This uneven division results in an averaged divide ratio of 3.2. Producing fractional division ratios allows higher comparison frequencies to be used while still maintaining narrow channel spacing requirements. Higher comparison frequencies reduce the feedback divide ratio, which in turn reduces the in-band phase noise. The drawback to this technique is the introduction of fractional spurs, which produce strong spurious noise. In the simple accumulator example cited here, these spurs would occur at $f_{comp}/5$ multiples from the carrier frequency, based on the fractional denominator. Delta-Sigma modulators spread the fractional spurs in an attempt to push them outside the closed-loop bandwidth of the PLL, where they are filtered from the output to a reasonable extent.

Prior to the advent of integrated-circuit technology, PLL systems were typically composed completely of analog circuits, whose operation could be described using linear feedback theory. The mixed signal solution shown in Figure 10 became the preferred embodiment for frequency synthesis as increased integration capabilities improved power consumption, area, and performance. Digital frequency dividers allowed for greater reconfigurability as well as the fractional-N techniques described previously. The analog phase detector typically implemented as a mixer circuit was replaced by the digital phase/frequency detector (PFD) that generally eliminated the need for acquisition circuits by having a pull-in range across the entire 2π range of potential phase offsets. The PFD was complemented by the charge pump circuit, which conserved power by allowing the loop filter to be implemented as a passive

circuit rather than the more power hungry active op-amp loop filter.

Despite the evolution from a purely analog to a mixed signal circuit, the linear design equations are still applicable under many typical operating conditions. The open loop gain of the PLL system from the input of the PFD to the output of the feedback divider can be expressed as

$$G_{OL}(s) = K_d F(s) \frac{K_{VCO}}{s} \frac{1}{N}, \tag{25}$$

where K_d is the PFD/charge pump gain, $F(s)$ is the loop filter transfer function, and K_{VCO}/s is the VCO transfer function after integrating the linear frequency control relationship of the circuit resulting in adjustments to the VCO output phase. The closed loop transfer function from the reference source to the PLL output is given as

$$H(s) = \frac{G_{OL}(s)}{1 + G_{OL}(s)} = \frac{\omega_n^2 \left(1 + \frac{2\zeta}{\omega_n} s\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{26}$$

The final form of (26) represents the characteristic equation of a second order system with two left-hand poles and a loop stabilizing zero. The variable ω_n represents the natural frequency of the system, which is equivalent to the reciprocal of the time it takes the signal to traverse the loop. Meanwhile, ζ represents the damping factor that characterizes the time it takes the loop to stabilize in response to a step change. For the loop filter shown in Figure 10, ω_n and ζ are derived in [14] as

$$\omega_n = \sqrt{\frac{K_d K_{VCO}}{N(C_1 + C_2)}} \tag{27}$$

$$\zeta = \frac{1}{2} \omega_n R_2 C_2 \tag{28}$$

The preceding theory represents the backbone of modern frequency synthesizer design. There are numerous permutations and clever techniques to improve various aspects of design performance, several of which will be explored in the following chapters.

1.3 SiGe BiCMOS Frequency Synthesis

Silicon-Germanium integrated-circuit platforms provide high performance devices comparable to other III-V compound semiconductors with the scalability and manufacturing of Silicon. For this reason, SiGe technologies are almost exclusively offered as a combination of high performance HBTs with standard MOSFETs known as BiCMOS processes. This combination is a powerful enabler for large scale integration of circuits with vastly different design requirements. The fundamentals of the semiconductor industry have demonstrated repeatedly that a greater amount of integration drives down the cost and size of electronics. This production advantage has led to wide-scale adoption of SiGe by nearly all of the major industry players in analog and RF integrated circuits.

Frequency synthesis for wireless and radar applications represents an ideal subsystem to take advantage of the strengths of SiGe process technology. The mixed-signal nature of the modern frequency synthesizer requires significant digital processing, as well as high-speed and low-noise performance from the analog and RF circuitry. These advantages have been recognized for many years and have been a significant factor in the development of SiGe since its inception. The research presented here explores several narrower aspects of frequency synthesis using the versatile SiGe platform. These can be categorized into investigations of unique application spaces, improving the advantages of the platform, and minimizing the drawbacks of the platform.

Extreme environment electronics represent an application space where SiGe devices can provide previously unconsidered advantages [19]. Extreme environments are most frequently encountered in space applications such as satellites or deep space probes where cryogenic temperatures and ionizing radiation present reliability concerns in traditional designs. The SiGe HBT has been shown to have improved tolerance to total ionizing dose over the traditional MOSFET. A variety of investigations are undertaken here to explore radiation hardening techniques for SiGe frequency

synthesizers. Additionally, speed and noise have been demonstrated as the primary advantages of the SiGe HBT. A number of designs and studies are presented that push the envelope of these performance specifications to maximize the advantages of Silicon Germanium. Finally, the linear operating region of a device is important for maximizing the dynamic range of a circuit. This is traditionally a weakness for the HBT relative to the MOFSET. In frequency synthesis applications, reduced linearity leads to lower oscillator output power and lock ranges for the closed loop system. An examination of AM/PM distortion is provided here in an attempt to reduce the impact of these effects.

CHAPTER II

PHASE NOISE MEASUREMENTS

Phase noise is a critical performance metric for most local oscillators in wireless communication and radar applications. However, obtaining accurate measurements of this parameter can be difficult and elusive with standard frequency domain measurement tools such as the spectrum analyzer. To demonstrate the cause of this difficulty, consider a sinusoidal signal in the time domain given by

$$v_o(t) = (A + \alpha(t)) \cos(\omega_c t + \theta + \phi(t)), \tag{29}$$

where $\alpha(t)$ represents amplitude noise and $\phi(t)$ represents phase noise. The variables A, ω_c, and θ represent the nominal amplitude, angular frequency, and initial phase offset respectively. Frequency is defined as the derivative of phase, which in this case is

$$\frac{d}{dt}(\omega_c t + \theta + \phi(t)) = \omega_c + \dot{\phi}(t). \tag{30}$$

Thus, the instantaneous frequency of the signal is a time-varying random function dependent on the phase noise, $\phi(t)$. Figure 12 highlights how the period uncertainty caused by $\phi(t)$ in (29) masks the value of the nominal frequency, ω_c, also known as the carrier frequency.

The physical sources of phase noise for a typical resonant-tank oscillator in integrated-circuit form are described in [75]. These processes produce a spectral noise power in a given bandwidth that is dependent on the carrier power as well as distance from the carrier frequency. The frequency dependence of this noise differs from thermal "white" noise sources whose spectral power density is constant across frequency. For

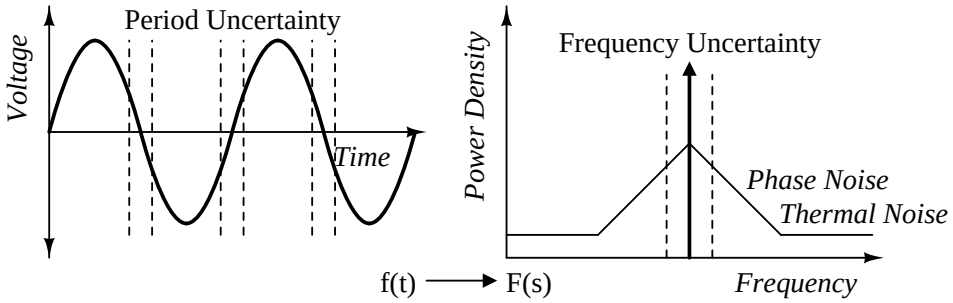


Figure 12: Uncertainty in the period of a time-domain sinusoidal waveform leads to uncertainty in the nominal carrier frequency as well, making an estimate of phase noise increasingly difficult at offsets close to the carrier.

this reason, phase noise is defined as spectral power relative to carrier power within a 1 Hz bandwidth at a specified offset from the carrier frequency. The units of this measurement are expressed as dBc/Hz. For example, a typical oscillator datasheet might specify a spot phase noise measurement of -100 dBc/Hz at 100 kHz offset from the carrier. An alternative specification typically shows a plot of phase noise values across offset frequency on a log scale. Note from the spectrum shown in Figure 12 that noise sidebands exist on both sides of the carrier. Phase noise is typically specified as the power contained within a single sideband (SSB) rather than the power contained in both sidebands, also known as double sideband (DSB). However, both specifications are equally valid, which leads many designers to explicitly state measurements as SSB phase noise or DSB phase noise to avoid confusion.

Understanding the phase noise specification highlights a number of reasons why the spectrum analyzer is a poor tool to measure this metric. Phase noise measurements depend on a precise understanding of the location and power of the carrier. However, (30) reveals that phase noise masks the true carrier frequency with time-dependent noise. Therefore, in order to capture reliable direct measurements of phase noise, the measurement would need to be instantaneous to prevent the carrier reference point from moving. A spectrum analyzer is a ubiquitous tool in electrical engineering for directly measuring spectral power by sweeping filters to measure spectral

power within a specified resolution bandwidth. As the resolution bandwidth of the measurement decreases, the measurement time increases accordingly. This confluence of a moving carrier target and increased measurement times makes phase noise measurements increasingly difficult as offsets get closer to the carrier. The spectrum analyzer also has no way of separating amplitude noise from phase noise shown in (29). For most applications this is not a concern as the amplitude-limiting mechanisms built in to an oscillator reduce amplitude noise to a level that is negligible compared to phase noise. However, there are situations where phase noise is low enough for amplitude noise to be non-negligible, and having the ability to separate these two noise sources can provide fundamental insight into physical noise sources as will be demonstrated in Chapter 3.

Despite these drawbacks there are a number of situations where the low cost and simplicity of direct phase noise measurements using a spectrum analyzer are desirable. Frequency variation of the carrier will be proportional to the RMS phase noise of the oscillator. Phase noise measurements taken at offsets much larger than this variation reduce the impact of the measurement uncertainties to provide reasonable estimates of phase noise. Similarly, very stable oscillators such as those phase-locked to a crystal can reduce the carrier variation and allow reasonable phase noise estimates even closer to the carrier frequency, although this fundamentally changes the phase noise characteristics within the servo bandwidth of the PLL. For these reasons, most commercial spectrum analyzers offer an expansion module for phase noise measurements. While these modules are suitable for some measurements, they can be quite constricting when trying to use phase noise as a tool to understanding device and circuit operation. A better measurement tool is needed, and the remainder of this chapter is dedicated to the system built to meet these demands.

2.1 Basic Principles

There are a number of different techniques to overcome the limitations of direct phase noise measurement described previously. All of these rely on the same basic back-end operation highlighted in Figure 13 [52]. Consider a mixer fed with two independent continuous-wave (CW) sinusoidal signals represented using the same construct as (29). Note that the nominal amplitude and frequency of each signal are considered equal so that only the phase offset and noise terms are independent. These terms give the time-domain response

$$v_{IF}(t) = \frac{(A_{LO} + \alpha_{LO}(t))(A_{RF} + \alpha_{RF}(t))}{2} \left[\cancelto{0}{\cos(2\omega_c t + \varphi_{sum}(t))} + \cos(\theta_{diff} + \phi_{diff}(t)) \right] \tag{31}$$

at the IF output of the mixer, where $\theta_{diff} = \theta_{LO} - \theta_{RF}$, $\phi_{diff}(t) = \phi_{LO}(t) - \phi_{RF}(t)$, and $\varphi_{sum}(t)$ is the sum of all of the θ and ϕ terms. The IF output thus contains two spectral tones, one at baseband and the other at twice the original carrier frequency. The low-pass filter shown in Figure 13 is used to discard the term at twice the carrier frequency, leaving only the baseband term for processing. Assume for the moment that the amplitude noise terms, $\alpha_1(t)$ and $\alpha_2(t)$, are small enough to be neglected. This approximation is suitable for most oscillators since amplitude noise is self-limiting [32]. However, we will explore the measurement possibilities if we intentionally violate this assumption in section 3.3 that analyzes distortion. The resulting operations and assumptions leave the following signal at the output of the low pass filter:

$$v_{IF}(t) = \frac{A_{LO}A_{RF}}{2} \cos(\theta_{diff} + \phi_{diff}(t)). \tag{32}$$

Using the filtered time-domain output of the mixer given in (32), we can now begin to use linear approximations to translate phase noise into voltage noise. These approximations will require that $\left| \frac{\phi_{diff}(t)}{\omega_c} \right| \ll 1$, which is reasonable for any useful

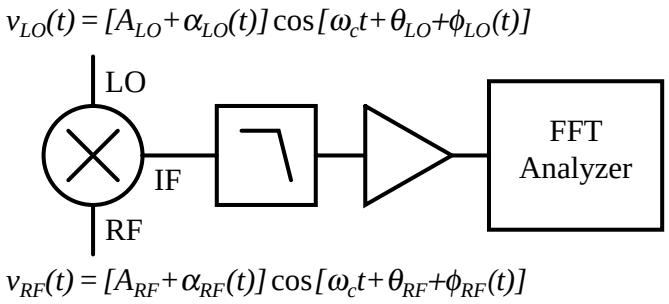


Figure 13: Mixing the oscillating signal to baseband is the key to eliminating carrier uncertainty.

oscillator. The problem can then be treated as a traditional small-signal analysis about a bias point determined by θ_{diff}. A plot of the bias function based on (32) can be seen in Figure 14. The optimal bias point for translating phase perturbations to voltage occurs at $\theta_{diff} = \frac{\pi}{2}$, a condition known as quadrature because it represents an orthogonal angle between two basis vectors in a two-dimensional Euclidean vector space. The small phase perturbation represented by $\phi_{diff}(t)$ about this bias point will have an approximately linear transformation to a voltage signal $v_{diff}(t)$ with a proportionality term, otherwise known as gain, determined by the slope of the bias function. This operation, which relies on the approximation that $\sin(x) \approx x$ for small x, can be written as

$$v_{diff}(t) = K\phi_{diff}(t), \tag{33}$$

where K is the mixer gain term, and will be critical in determining an accurate reference level for phase noise measurements. Mathematically, the mixer gain at quadrature is expressed as

$$K = \frac{d}{d\theta}\left(\frac{A_0^2}{2}\cos(\theta_{diff})\right)\Bigg|_{\theta_{diff}=\frac{\pi}{2}} = -\frac{A_{LO}A_{RF}}{2}, \tag{34}$$

which can be substituted into (32) to give

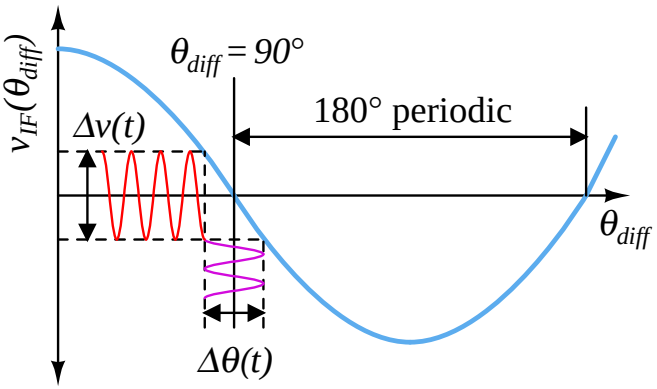


Figure 14: Ensuring that the RF and LO input signals to the mixer are in quadrature (90° offset in phase) allows a linear approximation translating phase noise to voltage noise. Leaving the signals in phase passes the amplitude noise through the mixer.

$$v_{IF}(t) = -K\cos(\theta_{diff} + \phi_{diff}(t)). \tag{35}$$

The resulting calculation of K allows several observations to be made. First, larger mixer gains will produce more sensitive measurements by virtue of allowing smaller phase perturbations to produce voltage signals large enough to be detected. Second, mixer gain will be directly determined by the amplitude of the carrier signal into the mixer, revealing that mixer drive level will be critical in determining the sensitivity of the measurement. A visual inspection of Figure 14 shows that quadrature is the optimum bias point that maximizes voltage swing for a given phase perturbation. However, we can also see that if the bias point is moved to an in-phase condition where $\theta_{diff} = 0$, the slope will go to zero and phase noise will be eliminated from the measurement. Applying this condition to (31) shows that the voltage output of the mixer will then become a direct measurement of the carrier amplitude and associated amplitude noise that was previously neglected. Finally, the optimal bias condition will occur periodically with a period of π because the bias function is sinusoidal. Since the variance of the measured noise will not change if the signal is inverted, the sign of the voltage output in (35) is irrelevant and any multiple of the quadrature condition

will produce the desired result.

Small-signal analysis has revealed how the mixer translates phase noise, $\phi_{diff}(t)$, to voltage noise, $v_{diff}(t)$, under the proper bias conditions. The remaining steps in the measurement involve amplifying the small voltage signal with a low noise and high gain amplifier, followed by translation to the frequency domain using a fast Fourier transform (FFT) analyzer. The FFT analyzer is essentially an analog-to-digital converter (ADC) that samples $v_{diff}(t)$ and performs an approximation of the Fourier transform to estimate the power spectral density in the frequency domain [6]. Since this sampling is of a signal converted to baseband from a carrier, the resulting frequencies computed by the FFT are the contents of the noise sidebands in terms of frequency offset from the carrier, f_m, as

$$S_v(f_m) = \int_{-\infty}^{\infty} |v_{diff}(t)|^2 e^{-\jmath 2\pi f_m t} dt. \tag{36}$$

Here, $S_v(f_m)$ is the power spectrum of the measured voltage in V^2/Hz. Note that (36) is typically calculated by the instrument and accounts for factors such as the measurement resolution bandwidth. This value is translated to DSB phase noise by substituting (33) into (36) to get

$$S_\phi(f_m) = \frac{S_v(f_m)}{K^2}. \tag{37}$$

Converting the DSB result of (37) to SSB involves dividing by two. Converting the SSB result to a decibel scale gives a final calculation of

$$\mathscr{L}(f_m) = 10\log(S_v(f_m)) - 20\log(K) - 3. \tag{38}$$

Note that these measurements obtain their value from $\phi_{diff}(t)$, which is a combination of the phase noise sources presented to the mixer in Figure 13. There are two approximations that can be made here. In the first, one signal source has significantly greater stability, and hence lower phase noise, than the other. For example,

suppose $\mathrm{Var}(\phi_{LO}(t)) \gg \mathrm{Var}(\phi_{RF}(t))$. In this case, $\phi_{RF}(t)$ becomes negligible and $\phi_{diff}(t) \approx \phi_{LO}(t)$. The oscillator supplying $\phi_{RF}(t)$ is considered a reference oscillator in this situation, as it supplies the necessary signal to stabilize the carrier, but does not contribute to the phase noise measurement. In the second situation, $\mathrm{Var}(\phi_{LO}(t)) \approx \mathrm{Var}(\phi_{RF}(t))$ and neither signal can be discarded. Here, we can say

$$\mathrm{Var}(\phi_{diff}(t)) = \mathrm{Var}(\phi_{LO}(t) - \phi_{RF}(t)) \approx 2\,\mathrm{Var}(\phi_{LO}(t)) \tag{39}$$

as long as $\phi_{LO}(t)$ and $\phi_{RF}(t)$ can be considered independent. The variance of an ergodic random variable can be estimated as [85]

$$\mathrm{Var}(\phi_{diff}(t)) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} |\phi_{diff}(t)|^2 dt, \tag{40}$$

which is equivalent to the total average power of the signal. Therefore, pushing the constant factor of 2 from (39) through the integral in (40) allows us to approximate that the power spectrum will double as well. In other words,

$$S_{v,meas}(f_m) = 2S_{v,osc}(f_m). \tag{41}$$

Repeating the derivation for $\mathscr{L}(f_m)$ from (37-38) reveals that a reduction of 3 dB from the measured spectrum will give an accurate estimate of SSB phase noise when both signal sources have comparable noise characteristics.

2.2 System Design Considerations

The system built to study phase noise for this research has been designed to be flexible for a variety of phase noise related measurements, and is fully documented online [39]. The system is designed to measure carrier frequencies between 500 MHz and 18 GHz and offset frequencies up to 10 MHz from the carrier. A system noise floor exceeding -170 dBc/Hz is targeted to accommodate the sensitive residual phase noise measurements desired. The entire system is placed on a cart for mobility allowing

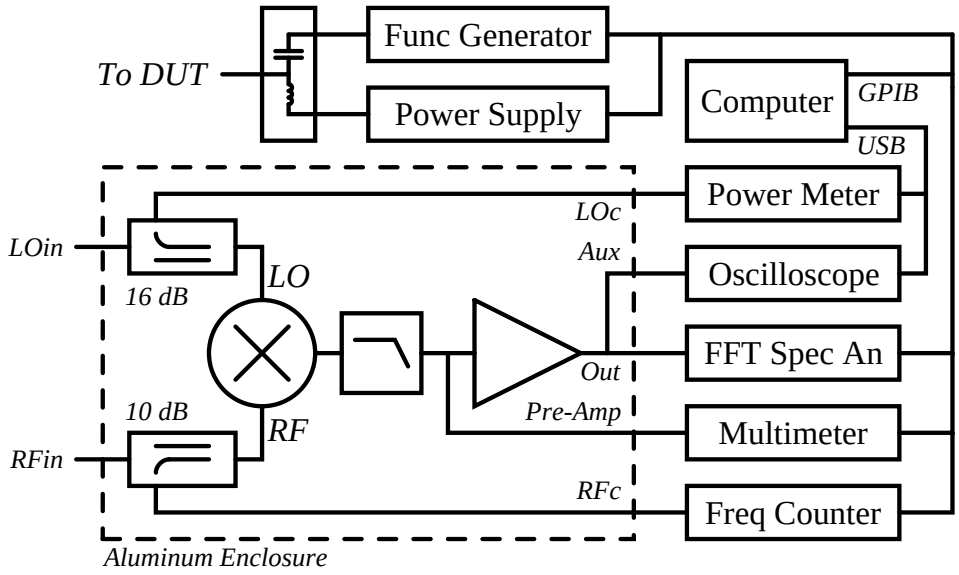


Figure 15: A system schematic of the fixed back-end of the phase noise measurement system.

it to be easily transported to other measurement stations as well as a shielded noise room. The back-end described in Figure 13 as well as other instruments required for test and calibration are shown in Figure 15. This equipment is fixed to the cart with interconnects converging on a custom aluminum enclosure as shown in Figure 16. A list of instruments used for this system are given in Table 1. The mixer is a Spectrum Microwave MM93PG-40 double-balanced design that covers the entire 0.5-18 GHz carrier range for the RF and LO ports with a nominal drive power of +7 dBm. The Krytar 1850 directional couplers cover the same band. The lowest drive option was selected for the mixer because this allows the system to be used with a minimum number of additional amplifiers to boost the power level and typically offers simplified designs that minimize potential DC offset and isolation problems [51].

Remaining components needed to implement the front-ends of the various measurement configurations can be reconfigured by the end user and placed in the staging area made up of the aluminum peg board shown in Figure 16. The peg board contains #4-40 tapped machine screw holes spaced on a one inch grid for custom mounting

Figure 16: A photograph of the phase noise measurement system without any front-end components.

Table 1: Measurement instrumentation used for the phase noise system.

Instrument	Model	Connection	Address
DC Power Supply	Agilent E3631A	GPIB	10
FFT Spectrum Analyzer	HP 89410A	GPIB	18
Frequency Counter	Agilent 53132A	GPIB	3
Function Generator	Tektronix AFG3252	GPIB	25
Multimeter	Agilent 34401A	GPIB	22
Oscilloscope	Tektronix TDS2012B	VISA	DPOUSB1
Power Meter	Agilent U2002H	VISA	EPMUSB1

needs. It is hoped that this configuration maintains maximum flexibility for measurements and encourages novel uses for the system while still being easy to use. Many of these front-end components do not cover the entire 0.5-18 GHz band, so multiple components are available depending on the desired measurement band. Table 2 lists the components available for use on the front-end at the time of this writing.

Table 2: Front-end components available for the phase noise system.

Component	Model	Frequency Band
Phase Shifter	RF-Lambda RFPSHT0004W2	DC-4 GHz
Phase Shifter	Spectrum GmbH LS-M018-2121	DC-18 GHz
Wilkinson Power Splitter	Narda 30183	1-18 GHz
Resistive Power Splitter	Agilent 11636B	DC-26 GHz
10 ns Delay Line	California RF	DC-18 GHz
25 ns Delay Line	California RF	DC-18 GHz
100 ns Delay Line	California RF	DC-18 GHz
Low PN Amplifiers (2)	Spectrum Microwave BX9327PM	0.1-2 GHz
Low PN Amplifiers (2)	Hittite HMC-C050	2-18 GHz
Variable Attenuator	Agilent 8494B	DC-26 GHz
Fixed Attenuators (8)	Mini-Circuits BW-SxW2+	DC-18 GHz
Isolators (2)	Pasternack PE8300	1-2 GHz

2.2.1 Baseband Amplifier

The baseband amplifier and low-pass filter shown in Figure 15 are critical for achieving noise floor and offset bandwidth desired for this system. No acceptable off-the-shelf solutions were available, so a custom design was implemented. This design was based on the National Semiconductor LMH6629 SiGe op-amp that delivers a 900 MHz gain-bandwidth product along with a 1600 V/µs slew rate to allow large gains out to the full 10 MHz offset bandwidth of the system. The part also features a 0.69 nV/$\sqrt{Hz}$ input-referred noise voltage to prevent excessive degradation in signal-to-noise ratio during amplification. This performance is unparalleled and is another indication of the diversity of applications for which SiGe technology can push performance limits.

Figure 17 shows the schematic for the baseband amplifier design. The RC low-pass filter passes frequencies up to 10 MHz with a small voltage drop across the resistor. Beyond the corner frequency, the capacitor becomes a virtual electrical short so that the input impedance seen by the IF port of the mixer becomes 50 Ω. A proper termination for the mixer at twice the carrier frequency improves the sensitivity to phase noise that overcomes the passband loss [43]. Coupling from the mixer to the amplifier is selectable by the user through a double pole, four throw (DP4T) switch. Available configurations are DC coupling through a buffer amplifier, or AC coupling with several low frequency cut-off values including 100 Hz, 1 kHz, and 10 kHz. DC coupling allows measurements down to arbitrarily low offset frequencies, but introduces more noise than AC coupling because of the necessary buffer.

A first stage gain of 30 dB with two op-amps in parallel provides the lowest noise figure possible. Surface mount metal film resistors and ceramic capacitors are used to achieve minimum excess noise through the passive components. The second gain stage provides selectable gain for final amplification to the instrument. The HP 89410A FFT spectrum analyzer used in the designed system has a large dynamic range for input signals, but the additional gain in the baseband amplifier increases

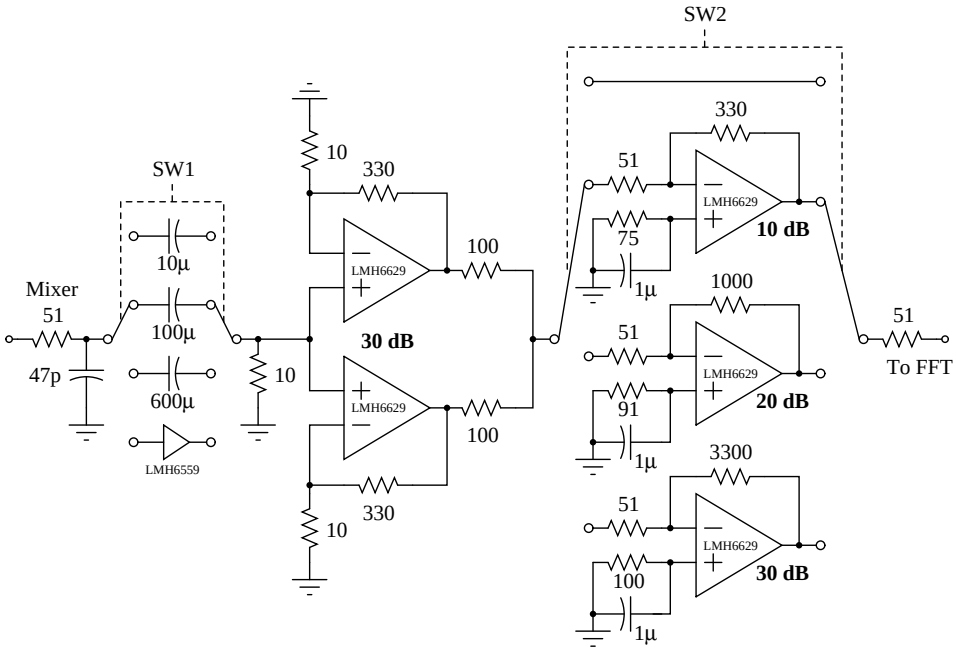


Figure 17: Circuit schematic of the low noise baseband amplifier.

the noise sensitivity proportionally. Total gain settings of 30 dB, 40 dB, 50 dB, or 60 dB are available through the baseband amplifier. The circuit hardware designs and enclosures are released under the creative commons attribution-sharealike 3.0 license (CC BY-SA) with material available at [39].

2.2.2 Interface Software

A comprehensive user interface is available for conducting phase noise measurements in the MATLAB environment. The software controls the various instruments using SCPI syntax through GPIB and VISA hardware addresses described in Table 1. The requirements to run the software are MATLAB 2009a or greater with the instrument control toolbox, as well as the National Instruments 488.2 drivers for GPIB communications using the National GPIB-USB-HS GPIB controller and the Agilent IO Libraries to control the USB power meter. Within the research group, the software is maintained and upgraded through a Subversion revision control repository along with other MATLAB instrument control routines, which allows dynamic growth for

the system from any member of the research team. A snapshot of this software as well as more detailed documentation is available under the CC BY-SA license at [39].

The software can be operated through two mechanisms. The fundamental phase noise measurements, calibration, and setup routines are conducted through a custom-defined class structure, phasenoise.m, which can be accessed from the command line or through custom scripts. A more user-friendly approach is through the graphical user interface (GUI), PN_CAPTURE.m. This GUIDE-based routine interfaces with the class structure directly and attempts to make the complex calibration and measurement requirements as simple as possible for the end user.

2.3 Two Oscillator Measurements

The next several sections discuss the various front-end configurations for the phase noise measurement system and the calibration techniques available to get an accurate measurement. The easiest method to practically implement the basic principles outlined in section 2.1 is to use two separate oscillators. This technique is useful for measuring phase-locked oscillators that can share a common reference frequency, and can be used to measure free-running oscillators when combined with a phase-locked discriminator. Two oscillator measurements are not used for this research, but they provide a useful exercise for system calibration that merits a brief discussion here.

The front-end configuration for a two oscillator measurement is shown in Figure 18, interfacing with the fixed back-end of Figure 15 through the $LOin$ and $RFin$ ports. Statistical independence of the noise is ensured by using physically separate oscillators, while phase-locking to common reference frequency ensures identical carrier frequencies. A phase shifter sets the appropriate θ_{diff} bias point between the two oscillators. This method is most effective in a "three-corner hat" configuration that measures the phase noise of similar ultra-stable oscillators [94]. In this approach, the noise power measured by the FFT spectrum analyzer will be double the noise power

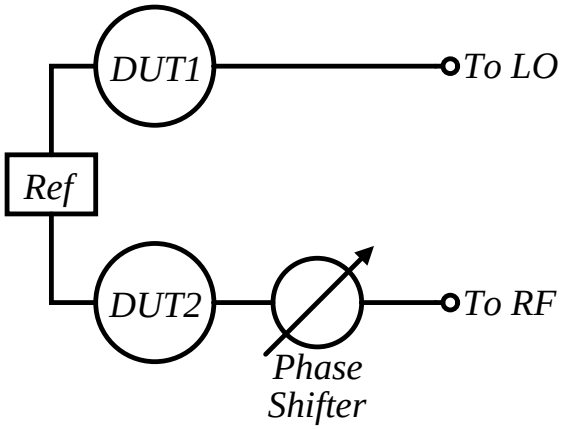


Figure 18: Front-end configuration for a basic two oscillator measurement. This method works best for measuring similar phase-locked synthesizers that share the same reference frequency.

of a single DUT, since both are similar. A 3 dB correction factor is therefore needed to estimate the noise power of a single DUT.

2.3.1 Beat Frequency Calibration

Two oscillator measurements have the simplest calibration requirements, which makes it a useful exercise for troubleshooting the designed system even if it is not required for any of the actual measurements presented here. With both oscillators operating at the same frequency, measured phase noise can be achieved using the procedure described in section 2.1. In order to make accurate measurements, the mixer gain, K, needs to be known beforehand. The mixer gain will be dependent on offset frequency from the carrier, as well as other factors such as drive levels and carrier frequency.

In the two oscillator measurement, the mixer gain can be determined by changing the carrier frequency of one oscillator from ω_c to ω_{coff}. The difference in carrier frequency will create a beat frequency at the output of the mixer, $\omega_{diff} = \omega_{coff} - \omega_c$. The sinusoidal beat frequency can be measured from the oscilloscope at the auxiliary output in Figure 15. The slope of the bias function at quadrature is determined by the amplitude of the carrier wave as demonstrated in (34), assuming the mixer

is operating with negligible distortion. This implies that K can be determined by measuring the peak voltage of the beat frequency on the oscilloscope. In practice, a peak-to-peak measurement is preferred to eliminate the influence of any small voltage offsets from the amplifiers, which is divided by two to give K.

The beat frequency calibration technique is an elegant and simple solution for calibration because it inherently accounts for any system losses before the mixer. By placing the oscilloscope after the amplification stage, beat frequency calibration also eliminates the need to include separate amplifier calibration, as that gain will be included in the measurement as well. However, the oscilloscope load in parallel with the FFT spectrum analyzer degrades the system noise floor performance, so care should be taken to remove the oscillator from the circuit by toggling the auxiliary output switch before measurement.

Consider the following procedure for conducting a two oscillator measurement using beat frequency calibration:

1. Connect the front-end of Figure 18 to the back-end system of Figure 15 and turn everything on.

2. Set the gain and low frequency roll-off to the desired settings based on the necessary noise floor for the measurement. Set the DUT carrier frequency to the desired value and set the DUT output power to be approximately +7 dBm at the mixer's LO input as measured by the USB power meter.

3. Establish the quadrature condition by adjusting the phase shifter and monitoring the multimeter until it reaches 0 V.

4. Connect the auxiliary output. Adjust the frequency of $DUT2$ to be ω_{diff} offset from the nominal carrier.

5. Visually confirm that the oscilloscope output looks sinusoidal so that the mixer

is not distorted. Measure the peak-to-peak voltage of the sinusoid and divide by two to get a mixer calibration term, $K(\omega_{diff})$.

6. Repeat 4 and 5 for as many offset frequencies as necessary.

7. Disconnect the auxiliary output, bring $DUT2$ back to the desired carrier frequency, and re-establish quadrature if necessary.

8. Measure phase noise and apply the calibration points by extrapolating between calibration measurements for the number of points captured by the FFT spectrum analyzer.

2.3.2 Phase-locked Discriminator

Measurements of free-running oscillators can also be made using the two oscillator method by phase-locking one oscillator via the error signal generated at the mixer's IF output. This technique is the favored method for most modern commercial phase noise test equipment [92,95]. These measurements are typically done with the phase-locked oscillator having much lower phase noise than the other oscillator so that it does not contribute to the noise measurement. The front-end and simplified back-end setup for these measurements are seen in Figure 19.

Although this method is not used for the present research, it can be implemented for the phase noise measurement system with the design of a simple plug-in module for the loop filter. Careful attention should be paid to the loop bandwidth of this system. Within the loop bandwidth the shape of the phase noise curve will be altered by the servo mechanism of the feedback loop [24]. However, beyond the loop bandwidth the phase noise characteristic is dominated by the oscillator. Therefore, a sufficiently narrow loop bandwidth will allow for carrier stabilization while still being able to observe phase noise close to the carrier. A good rule of thumb is that phase noise measurements for the oscillator become valid at an offset frequency one order of

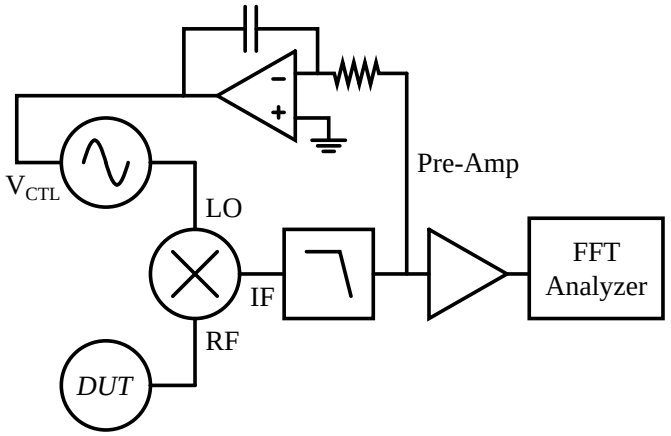


Figure 19: Measurement configuration for the phase-locked discriminator technique. This technique can be implemented for future measurements on the present system by designing a plug-in loop filter board to attach to the pre-amp output.

magnitude greater than the loop bandwidth. So in order to measure phase noise 1 kHz from the carrier, a loop filter that provides a loop bandwidth of 100 Hz should be designed.

A reference oscillator also needs to be provided to make this measurement. A "golden" oscillator based on the Crystek CVCO55BE covering 1-2 GHz is currently provided with the system as a means to troubleshoot the system using a VCO with known performance characteristics. This VCO should have sufficiently low phase noise to be a good reference for any solid state oscillators in this band. Measuring a DUT outside this band will require an additional oscillator part for the reference oscillator.

2.4 Single Oscillator Measurements

Single oscillator measurements make up a majority of the requirements for phase noise measurements and will be the focus of the work presented here. The techniques described here do not make up an exhaustive list of phase noise measurement possibilities. A notable exception includes injection-locking techniques [79]. However, it should be noted that any technique relying on baseband measurements as described

in section 2.1 can be measured on the system designed here by reconfiguring the front-end as necessary.

Single oscillator techniques will also be used to explore measurements beyond traditional phase noise of an oscillator. These include additive measurements such as residual phase noise and distortion measurements such as AM/PM distortion.

2.4.1 Residual Phase Noise

Residual phase noise measurements are conducted on two port circuits and provide a means to measure the phase noise degradation through the circuit block. This makes residual phase noise similar to a metric like noise figure, but applied to a signal exhibiting non-white noise and presented as a carrier-to-noise ratio rather than a difference in signal-to-noise ratios like noise figure. Residual phase noise measurements are critical for clock distribution circuits to preserve the signal integrity of high quality oscillators. This research will explore utilizing SiGe technology to improve residual phase noise performance in digital frequency dividers [38]. A similar measurement configuration will also be used to explore novel methods of understanding AM/PM distortion.

The front-end configuration for a residual phase noise measurement can be seen in Figure 20. The two port DUT is placed in the RF path. If the circuit under test is a linear time-invariant block, no identical block is needed for the LO path. However, if the circuit block alters the input frequency or produces a time-variant response, an identical circuit is required in the LO path to perform the same transformation and maintain the carrier dynamics required to accurately measure the phase noise. When two DUTs are present in the measurement, the noise output from each DUT can be considered equal and thus doubles the measured noise power. A 3 dB correction factor gives the equivalent phase noise of a single circuit. Without the second DUT in the LO path, the measured noise power is an accurate representation of the circuit

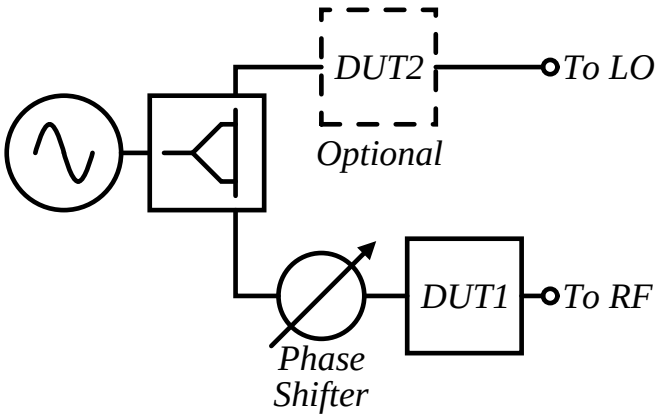


Figure 20: Measurement configuration for residual phase noise measurements. The second DUT in the LO path is required only if the DUT alters the input frequency of the carrier.

phase noise.

The signal source is a reference oscillator, which in this case is an Agilent E8257D signal generator. No remote commands are necessary for this instrument, so it is not necessary to connect it to the GPIB bus with the rest of the instruments. To make the measurement, the reference signal source is split with a power divider into two identical copies. These identical copies will have correlated signals and noise. Assuming no DUT is present in either the RF or LO branch, these signals will combine at the mixer in quadrature from the phase shifter unaltered. Since the noise is correlated it will cancel out when combined at the IF output of the mixer. Recall from (32) that the phase noise is embodied in ϕ_{diff}, which is the difference of noise from the RF and LO paths. Thus, if this random noise is strongly correlated, $\phi_{diff} \approx 0$.

The noise cancellation of the reference source gives an excellent system noise floor for measuring sensitive metrics such as residual phase noise. With the DUT in place, the noise output of the circuit will be uncorrelated from any of the other system noise. The noise of the DUT can then be measured as long as it is greater than the system noise floor. Making a measurement without the DUT in place is a way to determine this noise floor.

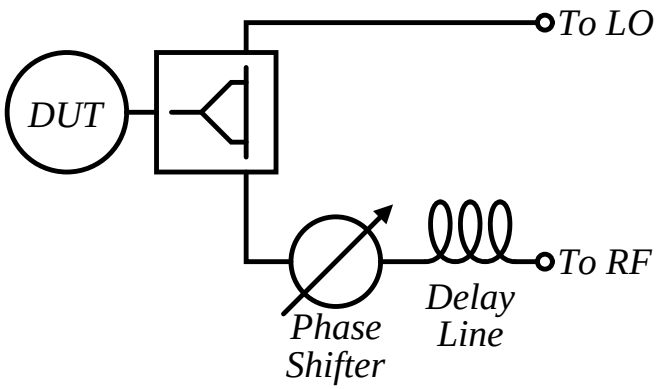


Figure 21: Measurement configuration for the delay line discriminator technique.

2.4.2 Delay Line Frequency Discriminator

Traditional measurements of signal source phase noise are also possible using a single oscillator. This work focuses on a delay-line frequency discriminator to complete this task. This technique is used in Section 3.1 to ascertain device level differences between *npn* and *pnp*-based oscillator circuits [40]. The front-end configuration for a delay-line measurement is shown in Figure 21. Note that this configuration is identical to the residual phase noise configuration with the exception of the delay line added to the RF path. The ultimate need for the delay line in this measurement is to un-correlate the noise so that it can be measured by the mixer [33]. However, this also has the effect of translating measurements of phase deviations into measurements of frequency deviations, requiring adjustments to the calculation of phase noise from these measurements.

White noise is by definition de-correlated, having an autocorrelation function that is a Dirac delta function at zero time offset. In other words, any shift in time alignment of the signal with itself (no matter how small) would cause the correlation to drop to zero. However, non-Gaussian low frequency noise is a fundamental component of phase noise. These noise characteristics are caused by memory effects, which produce a triangular autocorrelation function rather than the delta function exhibited by white

noise. This triangular function peaks at zero offset time and falls off symmetrically as the delay between the signals grows. Therefore, as the time shift between the two signal paths increases in the measurement setup, the de-correlation effect becomes greater and the measurement becomes more accurate.

Increasing the delay does not come without drawbacks, however. The delay line introduces significant loss, and increasing the delay increases this loss proportionally. Losses will also increase through the delay line as the carrier frequency increases. The power incident on the mixer needs to be large enough to drive the mixer and will directly contribute to the sensitivity of the measurement as seen in (34). This brings about an inherent trade-off between increasing delay to improve noise independence and decreasing delay to improve mixer drive. This is also the reason why the delay line is preferred in the RF path rather than the LO path. The RF mixer input typically has lower drive requirements for linear operation than the LO. The delay line should be non-dispersive so that the delay is constant across frequency. In this case, low loss coaxial line was cut to a variety of specified lengths and coiled to preserve space.

To understand how the delay-line transforms the measurement from a comparison of phase deviation to one of frequency deviation, consider the signal at the output of the mixer. Continuing with the formulation given in (29), this can be written as

$$v_{IF}(t) = A_{LO}\cos(\omega_c t + \phi_{LO}(t))A_{RF}\cos(\omega_c(t-\tau_d) + \theta_{diff} + \phi_{RF}(t-\tau_d)), \qquad (42)$$

where τ_d is the time delay through the delay line. Multiplying these terms and filtering out the high frequency term at $2\omega_c$ leaves

$$v_{IF}(t) = \frac{A_{LO}A_{RF}}{2}\cos(\omega_c\tau_d + \theta_{diff} + \underbrace{\phi_{LO}(t) - \phi_{RF}(t-\tau_d)}_{\text{Noise Term}}). \qquad (43)$$

Here, $\omega_c\tau_d$ will be a constant term at the carrier frequency of the measurement that combines with θ_{diff} to set the quadrature condition for the mixer. The highlighted

term in (43) represents the noise term that must be translated to a voltage to solve for the phase noise. However, unlike the other phase noise techniques discussed in this chapter where the delay between the RF and LO paths was small enough to consider the noise stationary, no such assumption can be made here.

Time domain analysis of this term is possible by using a Taylor expansion as shown in [26]. However, a more intuitive approach can be achieved by performing analysis in the frequency domain [80]. The Laplace transform can be used to separate the delay as

$$\phi_{IF}(s) = \mathcal{L}\{\phi_{LO}(t) - \phi_{RF}(t - \tau_d)\} = \phi_{LO}(s) - \phi_{RF}(s)e^{-s\tau_d}, \tag{44}$$

where $s = \jmath\omega_m$ corresponds with the offset frequency from the carrier. The LO and RF noise terms should now be identical and can be combined using the distributive property to give

$$\phi_{LO}(s) - \phi_{RF}(s)e^{-s\tau_d} = \phi_{VCO}(s)(1 - e^{-s\tau_d}). \tag{45}$$

This s-domain representation can be translated to a power spectrum by multiplying the signal with its complex conjugate. Thus, if we define $H(s)$ as the exponential term in (45), Euler's relation produces

$$H(s)H^*(s) = (1 - e^{-s\tau_d})(1 - e^{s\tau_d}) = 2(1 - \cos(\omega_m\tau_d)). \tag{46}$$

A final form for this term can be found by using the half-angle trigonometric identity to give

$$|H(f_m)|^2 = 4\sin^2(\pi f_m\tau_d). \tag{47}$$

The transfer function in (47) is the operation that transforms frequency fluctuations into phase fluctuations for the mixer. The function is periodic and non-linear,

which limits range of offset frequencies that can be measured using the delay line technique. For small frequency deviations, the same $\sin(x) \approx x$ approximation used in (33) can be used to give a linear transformation as

$$H(f_m) \approx 2\pi f_m \tau_d. \tag{48}$$

This approximation will hold reasonably well as long as $\pi f_m \tau_d \leq \frac{1}{2}$, and therefore the maximum offset frequency can be given as $f_m \leq \frac{1}{2\pi\tau_d}$. If higher order nonlinearities of the sinusoidal function are included, the maximum valid frequency offset can be increased to $f_m \leq \frac{1}{2\tau_d}$, but beyond this frequency the transfer function loses its monotonic characteristic and the resulting phase output becomes non-linearly aliased. Figure 22 highlights the transfer curve given in (47) for two lengths of delay line available for the constructed phase noise measurement system. Smaller delays will increase the offset frequencies capable of being measured, but at the same time will decrease the noise de-correlation provided, essentially limiting the sensitivity of the measurement.

An intuitive understanding of how the delay line transforms measurements of phase fluctuations to measurements of frequency fluctuations can be achieved as follows. Rewriting (44) and (45) in the s-domain yields

$$\phi_{IF}(s) = \phi_{VCO}(s)H(s) \approx -\jmath\tau_d s\phi_{VCO}(s). \tag{49}$$

The combination $s\phi(s)$ should be easily recognizable as the time derivative, $\dot{\phi}(t)$. The time derivative of phase is the definition of frequency. Therefore, the delay line transforms frequency fluctuations from the device under test into phase fluctuations at the mixer. These phase fluctuations are then transformed into voltage through traditional means.

With the transformation from frequency to phase complete, the remainder of the calculations to derive SSB phase noise proceeds similar to the process outlined

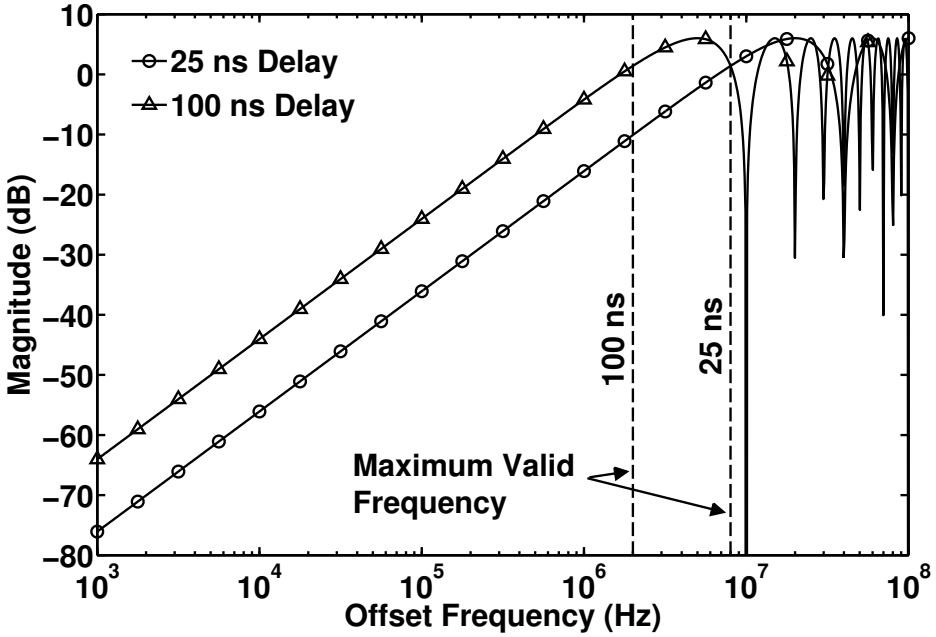


Figure 22: Plotting the delay line transfer characteristic for two different lengths of line. Linear approximations are valid until approximately 16% of the first null frequency at $\frac{1}{\tau_d}$. Nonlinear analysis can increase the valid range to 50% of the first null frequency.

in Section 2.1. Transformation from phase fluctuations to voltage fluctuations is identical to (37), which can be expressed as

$$S_v(f_m) = S_{\phi,IF}(f_m)K^2 = S_{\phi,VCO}(f_m)|H(f_m)|^2K^2. \tag{50}$$

From this point, back calculation of SSB phase noise can be given as

$$\mathscr{L}(f_m) = 10\log(S_v(f_m)) - 20\log(K) - 3 - 20\log(2\pi f_m\tau_d). \tag{51}$$

Note that (51) is identical to (38) with an additional term dependent on the offset frequency.

2.4.3 Single Oscillator Calibration

Determining the calibration factor for a single oscillator measurement is significantly more involved than a two oscillator calibration. This is due in large part to the carrier frequency being shared between both the LO and RF paths, making it impossible to create beat frequencies for calibration. However, there remain several creative solutions for making accurate measurements using a single oscillator. This section will highlight two such methods: a manual method that is simple yet involves several manual adjustment steps, and a more complicated modulation method that is more accurate and more capable of being automated.

2.4.3.1 Manual DC Calibration

The simplest method to calibrate a single oscillator measurement is to manually adjust the phase shifter to extrapolate the slope of the bias function shown in Figure 14. The procedure for such a calibration would happen as follows:

1. Connect the desired front-end configuration to the back-end system of Figure 15 and turn everything on.

2. Set the gain and low frequency roll-off to the desired settings based on the necessary noise floor for the measurement. Set the DUT carrier frequency to the desired value and set the DUT output power to be approximately +7 dBm at the mixer's LO input as measured by the USB power meter.

3. Establish the quadrature condition by adjusting the phase shifter and monitoring the multimeter until it reaches 0 V.

4. Adjust the phase shifter to a small but arbitrarily selected phase shift above quadrature, $\Delta\theta$, and record the voltage on the multimeter, V_1.

5. Adjust the phase shifter to the same $\Delta\theta$ below quadrature, and record the voltage on the multimeter, V_2.

6. Calculate the mixer gain, $K = \frac{|V_2 - V_1|}{2\Delta\theta}$.

7. Re-establish the quadrature condition for measurement and disconnect the auxiliary output if connected.

8. Measure phase noise and apply the single calibration factor to all measured points according to (38).

Note that if the multimeter is attached to the auxiliary output, the gain of the amplifier is included in the calculation of K. However, if the multimeter remains at the pre-amp output as shown in Figure 15, the amplifier gain needs to be included separately. The advantage of this calibration technique is its simplicity. The calibration can be done quickly with a simple calculator and no additional instruments other than a multimeter.

Despite this simplicity, there are several drawbacks that make this technique less than desirable. The first involves the low noise amplifier. In order to have an integrated calibration that includes the gain of the amplifier, the amplifier must be

DC coupled to the circuit. This option is available on the current system, but as established in section 2.2.1, DC coupling increases the amplifier's noise figure because of the buffer required at the input. DC calibration therefore reduces the effective sensitivity of the measurement system.

Another drawback is that the DC calibration cannot be extended across offset frequencies. The calibration factor will vary depending on the offset frequency, a factor easily seen using the beat frequency calibration technique for two oscillator measurements. The change from "nominal" conditions that one might calculate with the manual DC method occurs primarily at large offset frequencies above 1 MHz as parasitics begin to degrade the small signal gain in the system. The DC calibration method is also imprecise from a measurement perspective. Although the relevant voltages can easily be measured to four or five digits of precision, the phase shifters provide only coarse tuning capability and can really be determined to no more than one or two digits of precision. The lack of precise phase offset control leads to a larger variation in calibration factors and thus phase noise measurements. With careful measurement practices, the variation in phase noise measurements using this calibration method can be kept to within 1 dB.

2.4.3.2 Automated FM Calibration

A more accurate approach to single oscillator calibration uses frequency modulation (FM) to determine the calibration terms. This calibration technique can be used on any signal source that has FM capabilities. This includes measurements of voltage-controlled oscillators, where adjusting the voltage directly modulates the frequency of the DUT as well as residual measurements using a reference source with modulation capabilities such as the Agilent E8257D combined with option UNT. This method also requires a single adjustment of the phase shifter to quadrature, making

it much more conducive to automated calibration routines. The following derivation assumes a residual phase noise configuration shown in Figure 20. As demonstrated in section 2.4.2, the only change for a delay line measurement will be to add a $-20\log(2\pi f\tau_d)$ term to the final calculation of SSB phase noise in (38).

The calibration begins by applying an FM modulation to the signal source, which can be arbitrarily expressed as

$$v_{osc}(t) = A_0 \cos\left(\omega_c t + \int_0^t K_f m(\lambda) d\lambda\right), \tag{52}$$

where K_f is the modulation sensitivity in rad/V and $m(\lambda)$ is the modulated signal with λ being an independent time variable [27]. For the purposes of calibration, a simple sinusoid will suffice for the modulating signal, so we will set

$$m(\lambda) = A_m \cos(\omega_m \lambda). \tag{53}$$

Substituting (53) into (52) and integrating gives

$$v_{osc}(t) = A_0 \cos\left(\omega_c t + \frac{K_f A_m}{\omega_m} \sin(\omega_m t)\right). \tag{54}$$

With the basic form of the modulated signal source established, let

$$f_\Delta = \frac{K_f A_m}{2\pi}. \tag{55}$$

Here, f_Δ represents the maximum frequency deviation of the carrier in Hz by combining the modulation sensitivity with the peak modulating amplitude. The resulting signal source can be passed through the residual front-end of Figure 20 to give the following response at the output of the mixer with initial phase offsets normalized to the LO signal:

$$v_{IF}(t) = A_{LO}\cos\left(\omega_c t + \frac{f_\Delta}{f_m}\sin(\omega_m t)\right) A_{RF}\cos\left(\omega_c t + \theta_{\Delta c} + \frac{f_\Delta}{f_m}\sin(\omega_m t + \theta_{\Delta m})\right). \tag{56}$$

The amplitude and phase noise terms have been left out of these equations because they should play a negligible role in determining the calibration. Note that there are two phase offsets possible here, $\theta_{\Delta c}$ representing a phase offset of the carrier and $\theta_{\Delta m}$ representing a phase offset in the modulation signal. Carrying out the multiplication and filtering out the $2\omega_c$ term similar to (31) gives

$$v_{IF}(t) = \frac{A_{LO}A_{RF}}{2}\cos\left(\theta_{\Delta c} + \frac{f_\Delta}{f_m}\big[\sin(\omega_m t + \theta_{\Delta m}) - \sin(\omega_m t)\big]\right). \tag{57}$$

The term in square brackets from (57) can be rearranged using a sum-to-product trigonometric identity to give a more intuitive form at the mixer output as

$$v_{IF}(t) = \frac{A_{LO}A_{RF}}{2}\cos\left(\underbrace{\theta_{\Delta c}}_{\text{Bias Term}} \underbrace{+2\frac{f_\Delta}{f_m}\sin\left(\frac{\theta_{\Delta m}}{2}\right)}_{\text{Scaling Term}} \underbrace{\cos\left(\omega_m t + \frac{\theta_{\Delta m}}{2}\right)}_{\text{Time-Varying Term}}\right). \tag{58}$$

The form of (58) reveals several insights into the mechanisms of the FM calibration method. The sinusoidal FM modulation produces a corresponding sinusoidal deviation in phase about a bias point, $\theta_{\Delta c}$. This sinusoidal signal in phase is scaled by constant scaling term that helps ensure the phase deviation maintains small-signal assumptions for the modulating signal. This operation can be visualized in Figure 14 by the sinusoidal waveform bounded by $\Delta\theta(t)$. The time-varying term in (58) determines the offset frequency, $f_m = f$, for which the calibration term, $K(f)$, is valid.

The calibration will work by using the extents of the phase modulation to determine $\Delta\theta$ in Figure 14. This will be determined by the scaling term that determines the peak amplitude of the time-varying term. Since $\Delta\theta$ covers the peak-to-peak swing of the phase deviation, $\Delta\theta$ will be twice the scaling term. The extents of the oscillating

modulation are all that are needed for the calibration, so the temporal information is unnecessary. The phase offset in the time-varying term can therefore be dropped for simplicity. An estimate of the mixer gain can be completed by measuring the corresponding voltage deviation, Δv, using an oscilloscope attached to the auxiliary output. Like the phase deviation, the extents of the deviation are the only important information, so a peak-to-peak measurement function on the oscilloscope will give the desired metric. The mixer calibration can be completed from these measurements as

$$K = \left.\frac{\partial v_{IF}}{\partial \theta_{diff}}\right|_{\theta_{diff}=\frac{\pi}{2}} \approx \frac{\Delta v}{\Delta \theta}. \tag{59}$$

In order to accurately calculate the scaling term in (58) to produce $\Delta\theta$, a relation between the carrier phase offset, $\theta_{\Delta c}$, and the modulation phase offset, $\theta_{\Delta m}$, needs to be determined. This can be accomplished by relating each phase offset to the equivalent time delay. The signal delay through the front-end of the measurement system can be considered non-dispersive for any of the configurations presented here. The residual configuration will have much less delay between the RF and LO paths compared to the delay line configuration, but some finite amount of differential delay will still be present. The non-dispersive nature of each path means the delay for high frequency signals such as the carrier will be identical to that of low frequency signals such as the modulation waveform. Therefore, we can express the phase offset for the carrier as

$$\theta_{\Delta c} = 2\pi f_c \tau_{diff}, \tag{60}$$

where τ_{diff} is the difference in time it takes to arrive at the LO port versus the RF port from the signal source input in Figure 20. Likewise, the phase offset for the modulation signal can be written as

$$\theta_{\Delta m} = 2\pi f_m \tau_{diff}. \tag{61}$$

Substituting (60) into (61) gives a direct relation for $\theta_{\Delta c}$ and $\theta_{\Delta m}$,

$$\theta_{\Delta m} = \frac{f_m}{f_c}\theta_{\Delta c}. \tag{62}$$

This relationship can be substituted into the scaling term of (58) to eliminate the $\theta_{\Delta m}$ variable

$$\Delta\theta = 2\left(2\frac{f_\Delta}{f_m}\sin\left(\frac{f_m}{2f_c}\theta_{\Delta c}\right)\right). \tag{63}$$

The $\theta_{\Delta c}$ variable does not have much physical meaning when attempting to calculate the peak-to-peak phase deviation. There are two different methods that can be used to replace this value with one that is more easily measured. The first is to replace $\theta_{\Delta c}$ with its equivalent electrical length. This can be done because

$$\theta_{\Delta c} = \beta l_{diff} = \frac{2\pi}{\lambda_c}l_{diff} = \frac{2\pi f_c}{v_p}l_{diff}, \tag{64}$$

where l_{diff} is the difference in electrical length between the RF and LO paths in meters, λ_c is the wavelength of the carrier, and v_p is the phase velocity of the carrier. The total differential electrical length, l_{diff}, can be measured by combining physical measurements of hardline SMA cables used to connect the front-end components together along with electrical length conversions of the phase shifter reading in quadrature. For example, assume the front-end in Figure 20 used a 300 mm cable to connect the power splitter to the LO, and a pair 200 mm cables connecting the power splitter to the phase shifter and RF input respectively. Meanwhile the phase shifter reads 64° at the carrier frequency being measured. The total differential electrical length can be calculated as

$$l_{diff} = \left(0.2 + \frac{64^\circ}{360^\circ}\lambda_c + 0.2\right) - 0.3. \tag{65}$$

The calculation in (65) is sufficient to carry out the mixer gain calibration outlined

in (59). However, there is a second relationship for $\theta_{\Delta c}$ that can be exploited to reduce measurement uncertainties in l_{diff}. As shown in Figure 14, the bias function will be periodic with a period of π as any slope at the zero crossing will provide optimum sensitivity to phase noise regardless of sign. Valid values of $\theta_{\Delta c}$ can thus be restricted to

$$\theta_{\Delta c} = \frac{\pi}{2} + n\pi, n \in \mathbb{Z}. \tag{66}$$

If (66) is combined with the relationship in (64), a discrete expression for l_{diff} can be determined

$$l_{diff} = \frac{(2n+1)v_p}{4f_c}, n \in \mathbb{Z}. \tag{67}$$

Thus, measurements of l_{diff} only need to be accurate enough to determine the corresponding multiple of the bias function's zero crossing. Note that this will be inversely proportional to the carrier frequency. So while a margin of ± 53 mm might exist at a carrier frequency of 1 GHz, that margin of error shrinks to only ± 3 mm at a carrier frequency of 18 GHz. The final calculation for the mixer calibration can now be given in terms of l_{diff},

$$K \approx \frac{\Delta v}{\Delta \theta} = \frac{\Delta v}{4\frac{f_\Delta}{f_m}\sin(\frac{\pi f_m}{v_p} l_{diff})}, \tag{68}$$

or in terms of the zero-crossing multiple,

$$K \approx \frac{\Delta v}{\Delta \theta} = \frac{\Delta v}{4\frac{f_\Delta}{f_m}\sin(\frac{\pi}{4}(2n+1)\frac{f_m}{f_c})}. \tag{69}$$

Note that phase velocity is typically cited in the datasheet of an RF cable. Since this information was not available, a relative dielectric constant of 2.1 was assumed for transmission lines filled with PTFE. An automated routine to calculate (69) across

offset frequencies is included in the phasenoise.m class file under the autocal() method. A measurement utilizing this function would proceed as follows:

1. Connect the desired front-end configuration to the back-end system of Figure 15 and turn everything on.

2. Set the gain and low frequency roll-off to the desired settings based on the necessary noise floor for the measurement. Set the DUT carrier frequency to the desired value and set the DUT output power to be approximately +7 dBm at the mixer's LO input as measured by the USB power meter.

3. Measure the physical length of any cables used on the front-end configuration and enter into the software.

4. Connect the auxiliary output with the oscilloscope and the FM control line of the signal source to the arbitrary waveform generator and power supply combination.

5. Establish the quadrature condition by adjusting the phase shifter and monitoring the multimeter until it reaches 0 V. Enter the phase shifter reading into the software.

6. Select auto calibration. If the FM sensitivity, f_Δ in Hz/V, of the signal source is known, enter it manually. Otherwise let the software automatically calculate the sensitivity for the desired carrier frequency.

7. Once calibration measurements have completed, disconnect the auxiliary output and make sure modulation is disabled on the signal source. Re-establish quadrature if necessary.

8. Measure phase noise and apply the calibration points by extrapolating between

calibration measurements for the number of points captured by the FFT spectrum analyzer.

2.4.3.3 Modifications for Automated Calibration of Delay Line Measurements

The automated calibration routine derived in Section 2.4.3.2 is applicable for measurements of phase fluctuations such as the residual phase noise configuration and can even be used for measurements employing the phase-locked discriminator. However, measurements using the delay line discriminator measure phase noise by capturing frequency fluctuations as outlined in Section 2.4.2. In order to ensure that the automated calibration routine will work for these measurements, an understanding of the modifications introduced by this measurement technique must be developed.

The introduction of the delay line according to Figure 21 will alter the response of the RF path in (56) to be

$$A_{RF}\cos\left(\omega_c(t-\tau_d)+\theta_{\Delta c}+\frac{f_\Delta}{f_m}\sin(\omega_m(t-\tau_d)+\theta_{\Delta m})\right), \tag{70}$$

where τ_d is the time delay through the delay line. Carrying out the multiplication and filtering of (57) as well as the reorganization of (58) gives new values for the bias term,

$$\theta_{\Delta c}-\omega_c\tau_d, \tag{71}$$

as well as the scaling term,

$$2\frac{f_\Delta}{f_m}\sin\left(\frac{\theta_{\Delta m}-\omega_m\tau_d}{2}\right). \tag{72}$$

Using these new bias and scaling terms, it is possible to show that the relationship derived in (62) still holds unchanged recognizing that τ_{diff}, the difference in time delay betwwen the RF and LO paths, is not the same as τ_d, the time delay through

the delay line. Thus, a substitution of (62) into (72) can produce a new value for the peak-to-peak phase deviation,

$$\Delta\theta = 4\frac{f_\Delta}{f_m}\sin\left(\frac{f_m}{2f_c}\theta_{\Delta c} - \pi f_m \tau_d\right). \tag{73}$$

analogous to (63). The definition of $\theta_{\Delta c}$ remains unchanged, it is the phase offset of the carrier signal between the LO and RF path with no delay line. Therefore, the definitions in (64) still hold. Substituting these into (73) will give a new calibration calculation using l_{diff},

$$K \approx \frac{\Delta v}{\Delta\theta} = \frac{\Delta v}{4\frac{f_\Delta}{f_m}\sin(\frac{\pi f_m}{v_p}l_{diff} - \pi f_m \tau_d)}. \tag{74}$$

However, using the periodic restrictions on the bias point given in (66) changes the delay line result to

$$\theta_{\Delta c} - \omega_c \tau_d = \frac{\pi}{2} + n\pi, n \in \mathbb{Z}. \tag{75}$$

Substituting this value into (73) shows that the $\pi f_m \tau_d$ term cancels out, and the calibration calculation remains the same as (69). So ultimately the application of the calibration scheme will determine if modification is required to the calibration routine.

In order to make an accurate voltage measurement for the delay line auto calibration routine, it is important to remember the limitations the delay line places on the maximum offset frequency. Recall that for linear approximations to be valid $f_m \leq \frac{1}{2\pi\tau_d}$. Thus, in order to maintain accurate calibration measurements, $f_\Delta \leq \frac{1}{2\pi\tau_d}$. Recall that f_Δ is the peak frequency deviation of the calibration modulation that is a combination of the DUT sensitivity and the peak amplitude of the modulating source defined in (55). Since the sensitivity, K_f, is typically fixed for a given DUT, this implies that the amplitude of the modulating signal should be varied across offset frequency to produce the greatest voltage change without producing a non-linear

result that would distort the calibration. This relation can be expressed as

$$A_m \leq \frac{1}{K_f \tau_d} \tag{76}$$

CHAPTER III

NOISE AND LINEARITY STUDIES

The previous chapter highlighted the design and theory of a phase noise measurement system built for advanced phase noise studies of SiGe devices and circuits. This chapter will highlight the applications and studies for which the system was designed. These experiments cover a broad range of measurements. Beginning with a simple phase noise measurement of integrated oscillators, an effect is studied that shows unexplained differences in phase noise between identical oscillators implemented using complementary HBTs. An investigation of residual phase noise for frequency dividers is then explored using SiGe devices. These measurements are often overlooked and have been placed outside the capability of many modern commercial signal source analyzers that have sacrificed flexibility for ease of use. However, frequency dividers make up an important part of many clock distribution networks and can constrain the phase noise response in high-performance systems. Finally, studies in AM/PM distortion on SiGe devices are explored that push the boundaries of the phase noise system architecture. These types of measurements have not been attempted before and provide a number of opportunities to explore the boundaries of this technique.

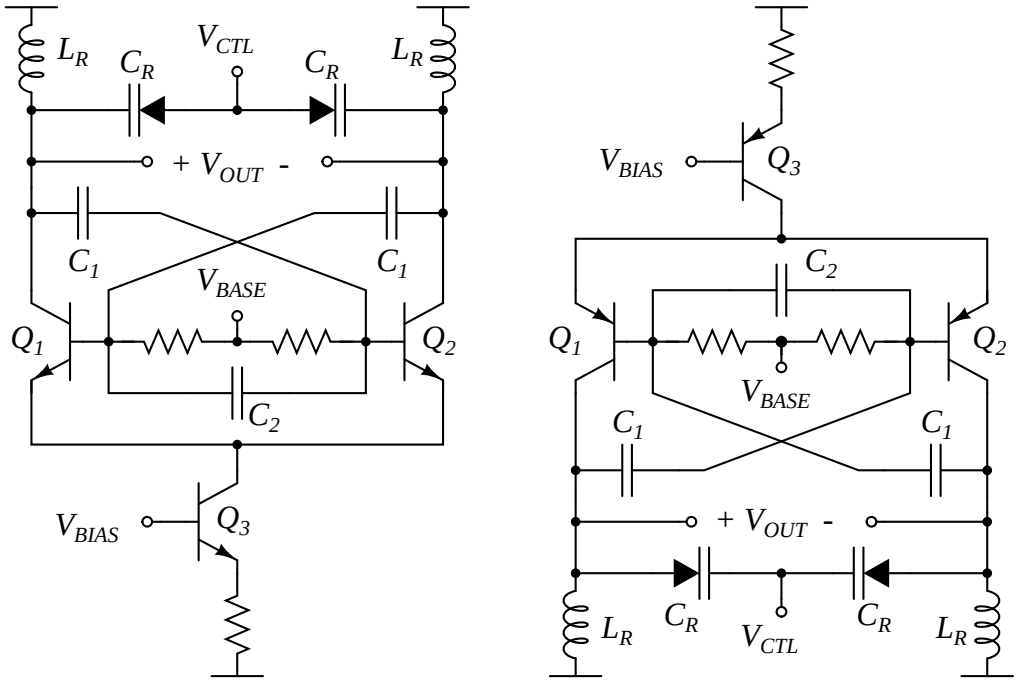
3.1 Phase Noise in Performance-Matched Complementary Oscillators

The performance advantages of the SiGe HBT and their implementation as a BiCMOS process have been outlined in Chapter 1. The majority of BiCMOS platforms use only a high performance *npn* SiGe HBT to reduce mask count, which keeps fabrication costs down. With only one device available, *npn* devices are preferred over

their *pnp* counterparts most notably for the higher carrier mobility of electrons relative to holes that gives *npn* HBTs a significant performance advantage. However, providing an additional high-speed *pnp* SiGe HBT can be advantageous to a number of applications [17]. For example, performance-matched (e.g., peak f_T) complementary SiGe HBTs can be used to reduce supply rails by creating bipolar folded-cascode stages. Due to the fundamental physical limitations of hole mobility and n-type valence band offsets in the *pnp*, matching performance typically requires "slowing down" the *npn* transistor after fine-tuning the germanium and doping profiles in the *pnp* for speed [98]. The desire for matched performance means that complementary SiGe platforms are typically a generation behind leading edge *npn*-only SiGe platforms.

This work examines a comparison of nearly identical voltage-controlled oscillators (VCOs) using both exclusively *pnp* HBTs and VCOs using exclusively matched-performance *npn* HBTs. These circuits were originally designed to benchmark a new low-cost BiCMOS platform, but phase noise observations that deviated from expected trends prompted further investigation. The results of this investigation were first published in [40], and raises interesting questions about the ideal characteristics of transistors for autonomous circuit applications.

The process under investigation is a complementary SiGe:C BiCMOS platform from IHP [35]. The 90 GHz f_T *pnp* and 100 GHz f_T *npn* devices were mapped onto a 0.25 µm third-generation platform also featuring a 200 GHz f_T high speed *npn*. Two identical oscillator designs were implemented in this C-SiGe platform, with schematics shown in Figure 23. The cross-coupled oscillator topology was chosen because it is both a very common integrated circuit design and allows direct bias control on the oscillating devices in the form of collector current and collector-base voltage (V_{CB}). The *npn*-only and *pnp*-only VCOs were designed identically in order to facilitate an investigation of the specific differences between the two types of devices. Both use an identical monolithically integrated resonator with an unloaded Q of 10.7 and use the



(a) *npn*-only (b) *pnp*-only

Figure 23: Schematics of the cross-coupled negative resistance oscillators used to develop this theory including an (a) *npn*-only design and (b) *pnp*-only design. For brevity, measurement data is presented for the *pnp* design only.

same device geometries. The frequency and amplitude response of both oscillators across control voltage can be seen in Figure 24. Parasitic capacitance has shifted the oscillators in opposite directions by approximately 8%, and the amplitude peak in the *pnp* oscillator represents an efficiency peaking at low control voltages.

The AC performance of the *npn* and *pnp* devices are shown in Figure 25 as a demonstration of the matched performance. This technology engineers the base and collector doping profile in the *pnp* to optimize heterojunction barrier effects. A novel collector design without deep trench isolation reduces parasitic capacitance and increases the overall speed of the vertical *pnp* [34]. The AC characteristics reveal that the unity current gain, f_T, is matched fairly well between the *npn* and *pnp*, although the *npn* still exhibits a noticeably higher maximum oscillation frequency, f_{max}. In addition, the complementary devices have almost identical output impedance at a

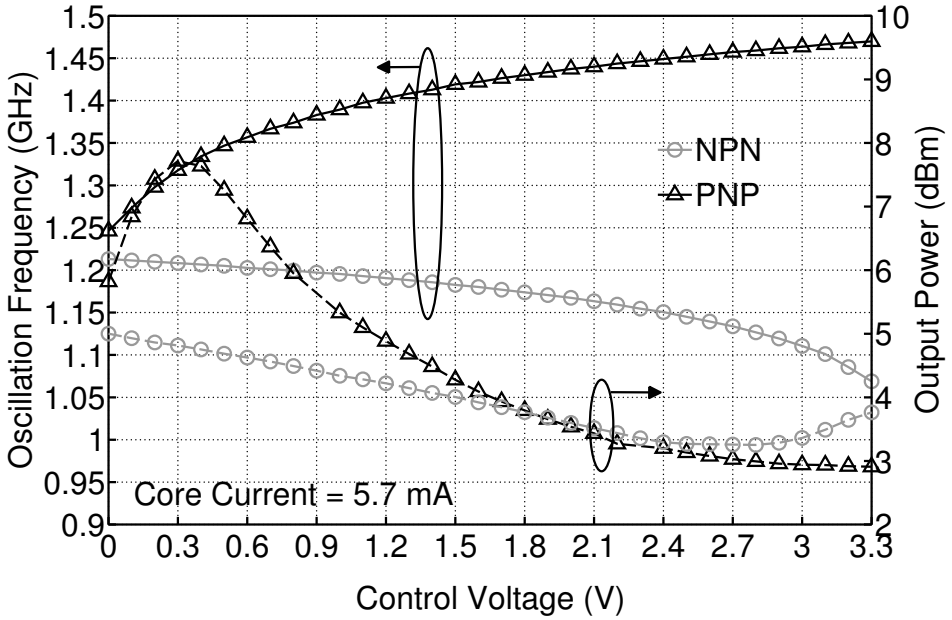


Figure 24: Frequency and ouput power characteristics of the *npn* and *pnp* oscillators across control voltage.

fixed collector current, seen in Figure 26. This fixed output impedance should ensure that the loaded Q of the resonators remains comparable for both the *npn* and *pnp* oscillators, as both use identical inductors and varactors, with the polarity reversed to ensure proper oscillation.

A comparison of low frequency noise is shown in Figure 27, and is referred to the "output" collector node of the device. The output-referred noise is used because in this topology it is the collector that is tied to the resonator of the oscillator, and through this node that device noise is coupled into the output signal. Figure 27 reveals that the *pnp* HBT has a significantly higher $1/f$ corner frequency than the *npn* HBT. Beyond the $1/f$ corner where thermal noise dominates, an S-parameter extraction of the base resistance shows the *pnp* resistance is around 250Ω while the *npn* base resistance is around 170Ω. In terms of noise power, this is a difference of $1.7dB$ in favor of the *npn* HBT. These characterstics lead to the hypothesis that the *pnp*-based oscillator should have a worse phase noise performance than the *npn*

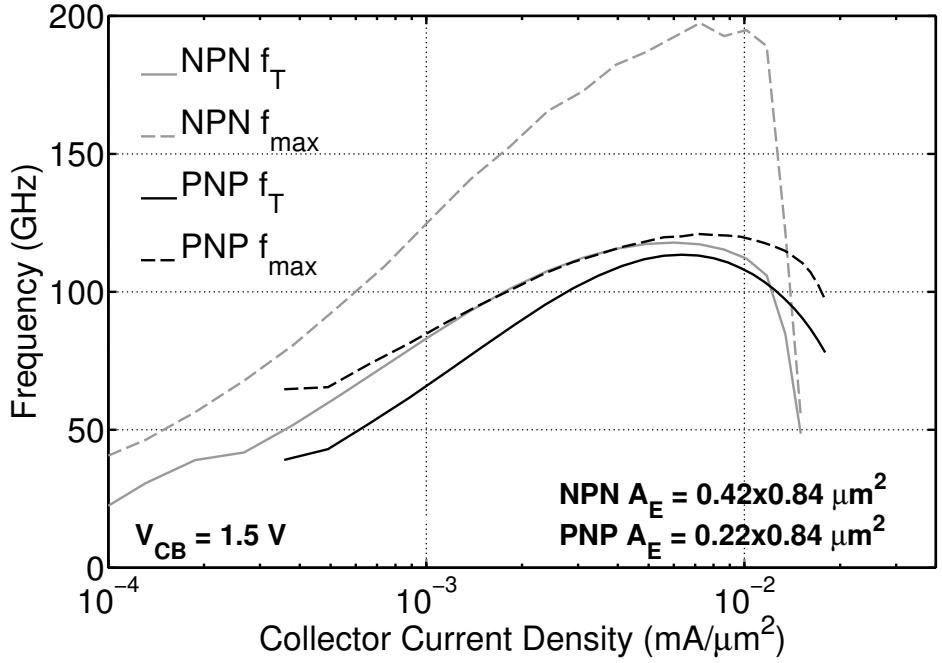


Figure 25: AC characteristics of the *npn* and *pnp* high-speed complementary SiGe HBTs in the IHP SG25H3 process.

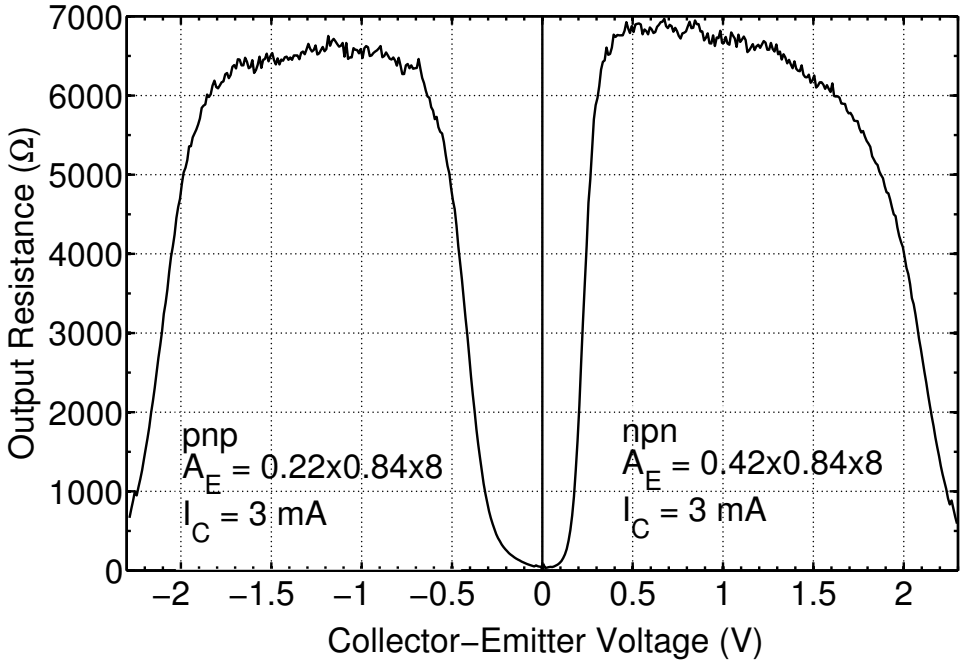


Figure 26: Output resistance of the *npn* and *pnp* high-speed complementary SiGe HBTs at constant collector current. Given the identical resonators used, this eliminates the possibility of varying resonator Q as the cause of the phase noise differences observed.

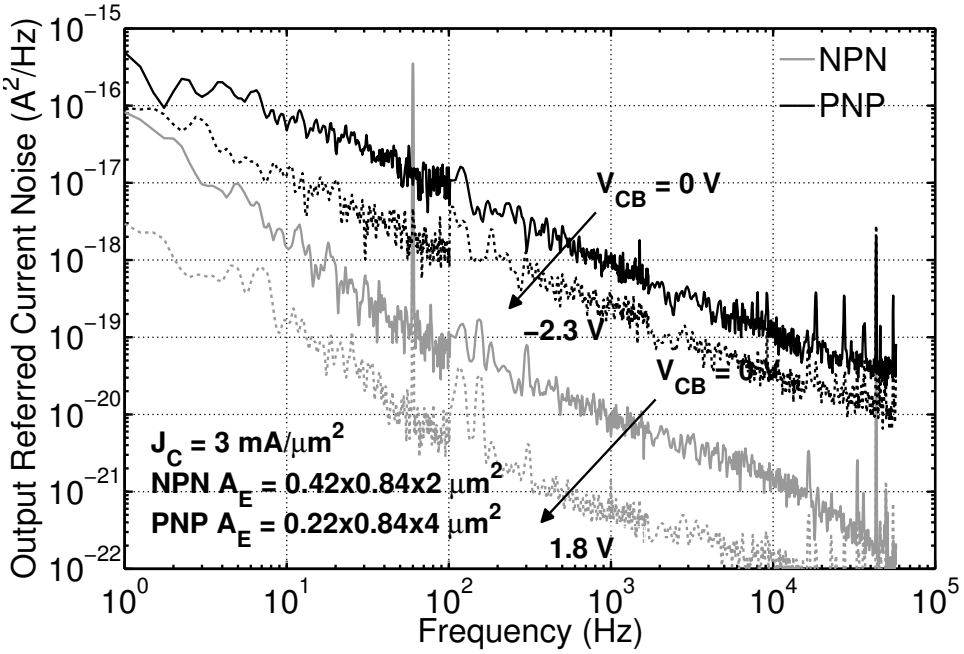


Figure 27: Measured low frequency noise of the *npn* and *pnp* devices. The *pnp* device displays a significantly higher $1/f$ corner frequency and thus a much higher noise level at low frequencies.

oscillator. Another critical difference lies in the DC current gain of the device. A forward Gummel characteristic reveals that the *pnp* HBT has a peak β of 200 versus 100 for the matched *npn* HBT.

3.1.1 Measured Phase Noise Performance

The phase noise of the free-running VCO designs was measured using the delay line configuration described in Chapter 2. Figure 28 shows the phase noise at a 1 MHz offset averaged across control bias and plotted across core current bias. The *pnp*-only circuit shows a mean phase noise improvement of up to 5 dB compared to the *npn*-only VCO beyond the threshold where the oscillators are fully turned on. This advantage cannot be associated with the higher output power seen in the *pnp*-only VCO at low control voltages. Figure 29 shows a plot of the phase noise at a constant 5.7 mA bias current and 1.5 V control voltage. Figure 24 shows only a 0.4 dB difference in output power under these conditions, yet at 1 MHz offset the *pnp* VCO still shows over 4 dB

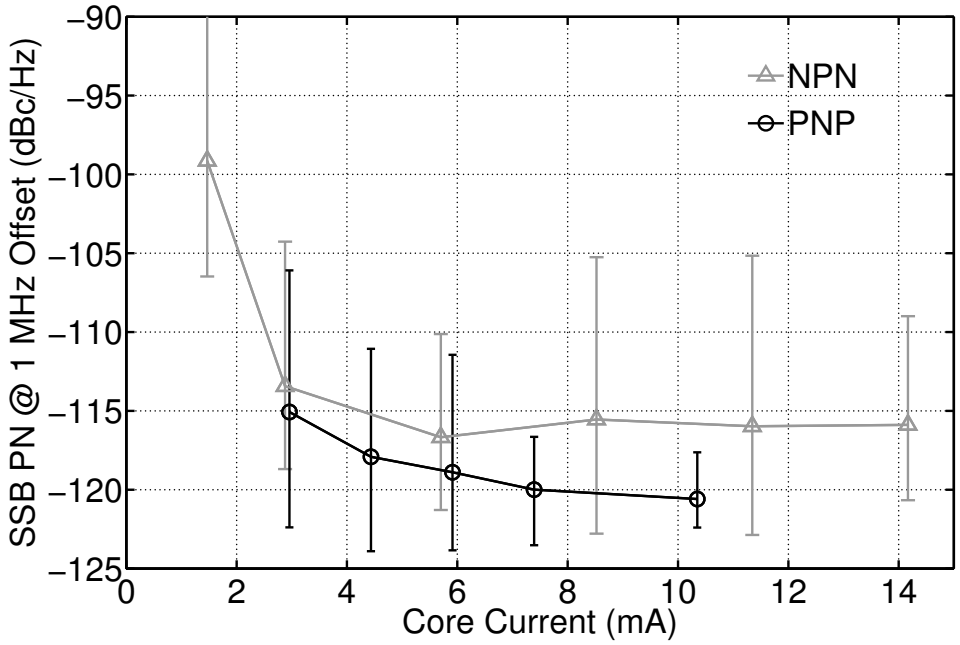


Figure 28: Measured phase noise of the VCOs across bias current. Error bars represent the high and low values of phase noise measured across the control voltage tuning range, while the markers represent the mean value. The large variation seen is a product of changing resonator Q across varactor bias as measurements are repeatable to within 1 dB.

improvement in phase noise.

The root cause of the improved phase noise for the *pnp* VCO can be traced to differences in the inherent DC current gain of the devices. To arrive at this conclusion, we start with Leeson's model for *a posteriori* analysis of phase noise given in [57] as

$$\mathcal{L}(\Delta f) = 10log\left(\frac{2FkT}{P_S}\left[1+\left(\frac{f_0}{2Q_L\Delta f}\right)^2\right]\left(1+\frac{\Delta f_c}{\Delta f}\right)\right) \tag{77}$$

where f_0 indicates the frequency of the carrier and Δf_c is the $1/f$ corner frequency of the device. Figure 29 reveals an f^{-2} slope in the region where the *pnp* VCO phase noise is lower, indicating an advantage for this device in a region outside the 1/f corner frequency of the device but still inside the bandwidth of the low-Q resonator in a region known as white FM noise. Note that Δf_c for the *npn* and *pnp* oscillators are denoted by black dots in Figure 29. The higher corner frequency of the *pnp*

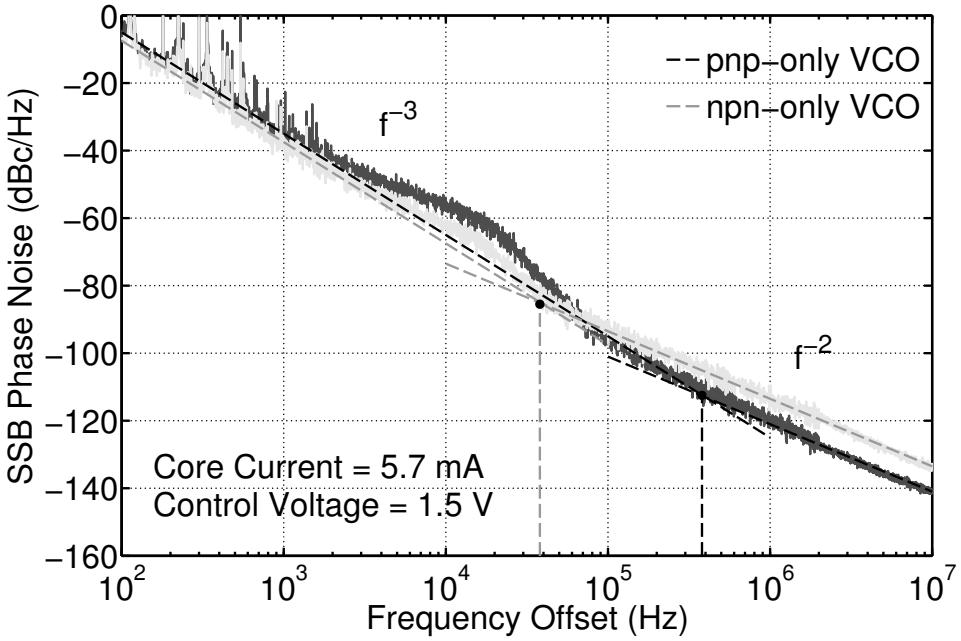


Figure 29: Measured phase noise of the VCOs at constant bias current and control voltage. Despite having higher phase noise at close-in frequency offsets due to a larger $1/f$ corner frequency, the *pnp*-based VCO displays significantly lower phase noise in the white FM region.

HBT does lead to higher noise at very close-in frequency offsets, which confirms the expectations taken from Figure 27. Thus, knowing that the oscillators have similar output power, P_S, and are using resonators with nearly identical Q_L, one can conclude that the difference in white FM noise is attributed to higher low frequency white noise in the *npn* circuit, the F factor in (77).

There are three primary sources of noise in a SiGe HBT: thermal noise from the base resistance, and shot noise from both the base and collector currents [21]. Because the base resistance is slightly higher in the *pnp* HBT, the thermal noise power will be roughly $1.7dB$ higher relative to the *npn* HBT. An analysis of the Gummel characteristics reveals that the matched *npn* device has a DC current gain (β) of 176 at the nominal 5.7 mA bias current of the VCO. In comparison, the *pnp* has a β of only 53 at this same bias point. In the small-signal hybrid-π model of the HBT shown in Figure 30, r_π is defined as the ratio between β and the transconductance,

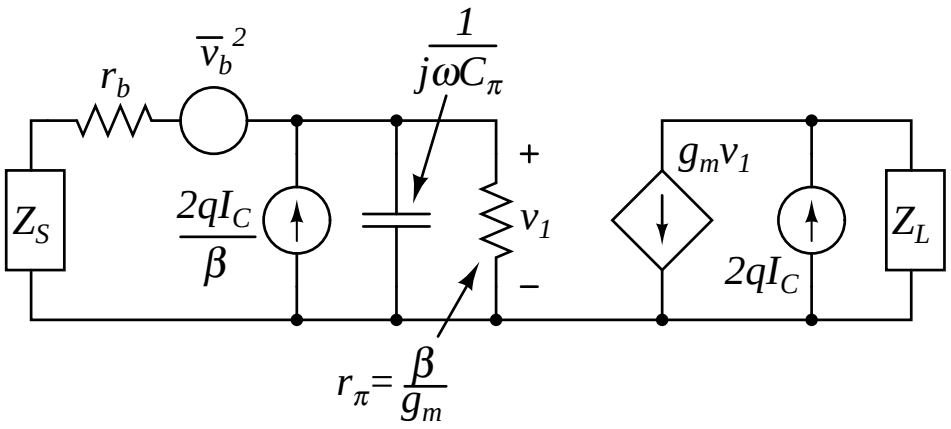


Figure 30: Small-signal noise model that leads to the difference in collector-referred noise in the matched *npn* and *pnp* devices at a constant collector current.

g_m, making r_π directly proportional to β at a constant collector current.

We assume that the collector current is held constant between the *npn* and *pnp* HBTs, and refer all noise sources to the collector node which is tied to the output node in the VCOs and will be the noise source when the device is "on". Since the collector current is constant, the shot noise in the collector will be identical. Base shot noise will also be identical since the increase in r_π will be offset by a corresponding decrease in base current by the same factor. However, the differential in r_b between the two devices is only a few ohms, meaning both have similar input-referred thermal noise levels. Hence, the increased β, and therefore r_π, of the *npn* device will result in more noise at the collector. This is because the ratio of r_π has increased relative to r_b and the collective source impedance, Z_S, that make up the remainder of the input voltage divider (see Figure 30). Keep in mind that although the base thermal noise is common to both "halves" of the symmetrical differential circuit, the noise is uncorrelated and hence will not cancel out as most common-mode signals would.

The inherent difference in β between the matched *npn* and *pnp* devices has been shown to lead to increased collector-referred noise in the *npn* HBT. The degree to which this change in β will affect the total white noise level is dependent on a number of factors, including I_C, r_b, and Z_S. However, the effect of C_π can be largely

neglected under most conditions (recall that we are interested in low frequency noise greater than the 1/f corner frequency but less than the bandwidth of the resonator). Specifically, our measurements have covered the 100 Hz to 10 MHz carrier offset range, and thus the corresponding spectral range of low frequency device noise will be up-converted. At these frequencies, the impedance of C_π will be large for most of the combinations of β and I_C that make up r_π, to first order. When these combine in parallel the effect of C_π can be neglected. This white low frequency noise then becomes white FM noise about the VCO carrier.

Simulations made by varying the input impedance suggest that a β difference from 200 to 100 could swing the phase noise as much as 6 dB relative to an otherwise identical device. Since the higher r_b of the *pnp* adds approximately 1.7 dB of input-referred noise, these results seem to indicate the *pnp* device should always hold some advantage over the matched *npn* for oscillator designs built in this platform. The effect seen here is distinct and repeatable, but further confirmation of the effect through an independent circuit is suggested to validate the presented theory and is in progress. Although the degree of phase noise improvement can be adjusted through circuit and bias adjustments, the fundamental change caused by variation in β seems to be real given the evidence available.

3.1.2 Analysis and Implications

The measured results of cross-coupled VCO designs in a C-SiGe process technology reveals that a *pnp*-only design yields superior phase noise performance to a performance-matched *npn*-only design. Using phase noise theory, the improved performance can be traced to a reduction in the white FM noise observed in the *pnp* design. A process of elimination leads to a theory attributing the reduced β of the *pnp* device as the source of the observed difference. These results are counter-intuitive because they are the opposite of what one might expect by only considering absolute base resistance

levels. In addition, lower β is typically seen as degrading performance in amplifier design.

The change in white FM noise observed in the phase noise spectrum has a significant impact on PLL design. When this type of noise dominates, free-running RF oscillators can show a significant random variance in frequency. This is a primary motivation for locking these signals to a much more stable reference for frequency synthesis. The white FM variance is an important parameter to understand for use in a PLL because it will determine the minimum loop bandwidth required to keep the oscillator locked. PLL loop bandwidth is inversely proportional to settling time and proportional to spur levels. White FM noise can be suppressed by reducing the noise level within the resonator bandwidth as demonstrated with the reduced β of the *pnp* or by increasing the Q of the resonator to reduce the spectral range with which this type of noise can accumulate. Since Figure 29 shows this particular noise characteristic is significantly larger for the *npn* VCO, it would be worthwhile to attempt to quantify its effect on a synthesizer design.

Measurements were taken on the VCOs by sampling the oscillation frequency over time using the spectrum analyzer. In this sense, the instrument was acting like a crude frequency counter. The gate time was approximately 1.5 ms. The raw measured results contain two types of frequency variance; deterministic and stochastic. Deterministic frequency drift caused by aging and warm-up is linear and can be removed to reveal the stochastic frequency variation [86]. This data can be seen in Figure 31 for the *npn* and *pnp* VCOs at a control voltage of 1.5 V. Both VCOs give Gaussian distributions, a clear indicator that white FM noise is dominating all other sources. The *pnp* VCO, with its reduced white FM phase noise, shows much less variance than its *npn* counterpart. The takeaway is that the inherent difference in β that gives the *pnp*-only VCO better noise characteristics also reduces the 3σ variation of the frequency to 19.5 kHz compared to 35.7 kHz for the *npn*-only VCO, a factor

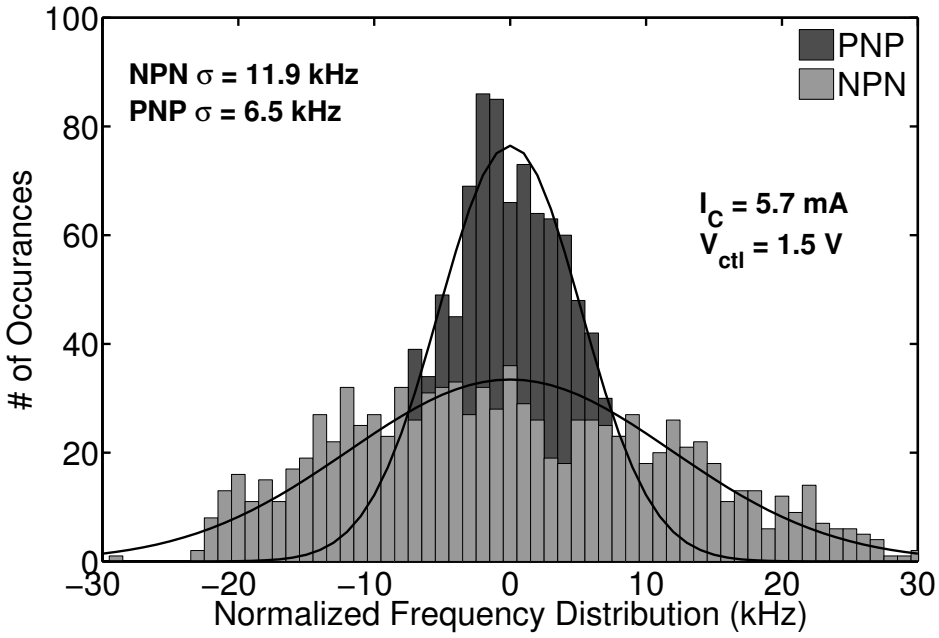


Figure 31: Random frequency variation of the *npn* and *pnp* oscillators normalized to the carrier frequency. The solid line is the ideal Gaussian distribution based on the variance estimator from the measured data.

of 2 improvement. In applications that demand a PLL with low noise spurs, this advantage could be significant.

The results observed in these measurements go beyond utilizing high-speed vertical *pnp* devices to get a few dB of oscillator phase noise improvement. Circuit techniques such as inductive degeneration can be used to level the playing field for the matched *npn* HBT, even though this would come with a significant die area penalty. Rather, the results may point to potential device optimization for low phase noise oscillators. Perhaps a reduced technology node with lower β would provide superior phase noise performance to a comparable design in a more advanced node of the same technology, provided the device f_T remained high enough. Perhaps the devices that are tailored to amplifier design are sub-optimal for autonomous circuits such as oscillators. Independent circuit verification of these results and an understanding of the limits of the proposed effect will ultimately decide if our observations can be exploited to provide meaningful insight into oscillator device selection.

3.2 Residual Phase Noise in Digital Frequency Dividers

Frequency dividers are useful tools to efficiently achieve the flexible frequency plans required of PLLs. In wireless systems, these circuits are most frequently found in LO synthesizers with the capability to be programmed digitally. By adjusting the division ratio, a voltage-controlled oscillator can produce many different spectrally-pure microwave tones when phase-locked to a reference oscillator. In this configuration, the division ratio of the frequency divider acts as a noise multiplier in the closed-loop response such that larger division ratios produce greater in-band noise levels [29]. Compared with these large multiplication factors, the residual phase noise through such dividers often produces a negligible impact on synthesizer output phase noise. However, the desire for increased functionality and flexibility has proliferated the use of frequency dividers to other areas of the synthesizer where residual phase noise becomes a greater concern for high performance systems.

Channel dividers are typically placed at the output of the synthesizer. They allow integer divisions of a single synthesized source, which in some applications can reduce the overhead of multiple synsthesizers through careful frequency planning. Because channel dividers are outside the feedback loop, they reduce the noise power by the division ratio. Therefore in low noise synthesizers, residual phase noise through a channel divider becomes critical as it represents the final noise floor limit. An example of a receiver employing a two channel synthesizer including a channel divider is shown in Figure 32. Here, the first synthesizer channel drives the LO port of the mixer for downconversion, while the second channel passes through the channel divider to drive the clock of an analog-to-digital data converter (ADC) for direct IF sampling. The dashed line shows the simulated phase noise of the synthesizer output that drives the mixer. At this performance level, a channel divider with a phase-noise floor of-155 dBc/Hz would limit the overall phase noise (or jitter in the time domain) of the clock signal driving the ADC. Improving the phase-noise floor of the channel divider to

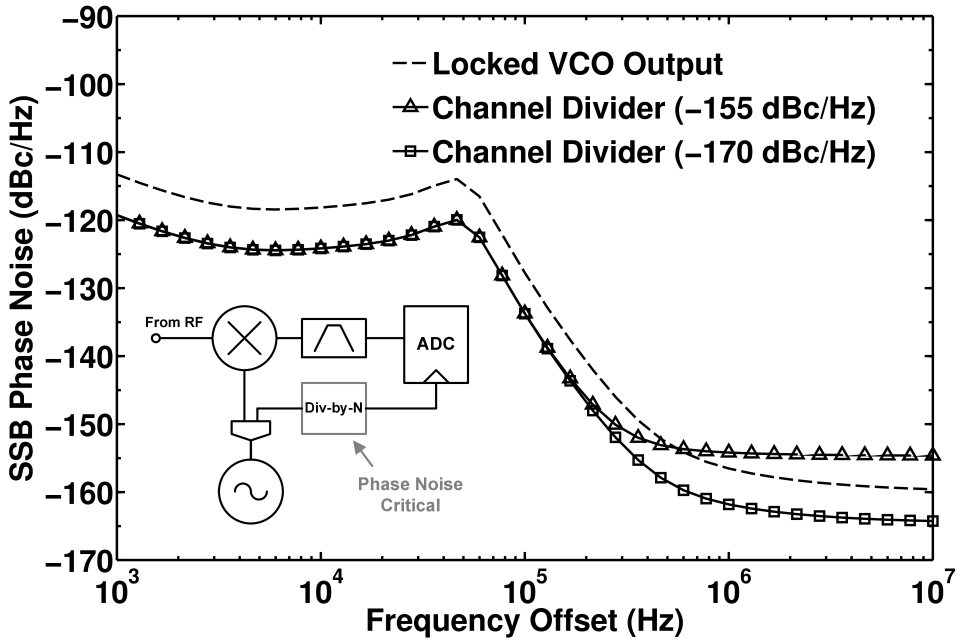


Figure 32: A simulated example of channel divider residual phase noise limiting the overall phase noise performance of a wireless communication system.

-170 dBc/Hz would allow a full realization of the noise-reduction benefits through the divider itself. This section pioneers methods of reducing phase noise by providing a separate bias to the storage cell of a current-mode logic (CML) digital latch, first presented in [38]. This method improved phase noise at the expense of frequency range by placing a lower frequency limit on the circuit caused by the necessity of series capacitors. Recent commercial offerings can now produce phase noise floors up to -163 dBc/Hz likely using a similar technique [1]. This effort is followed up by a complementary work examining a similar comparison using an output buffer on the flip-flops of the digital latch. The revised design seeks to exceed this performance while eliminating the operating frequency restrictions of previously developed designs.

3.2.1 Modified Latch Frequency Dividers

The basic building block of the high-speed digital frequency divider is the master-slave D latch. The latch is made up of two D flip-flops, as shown in Figure 33, cascaded together with anti-phase clock signals. For high-speed bipolar circuitry, these blocks

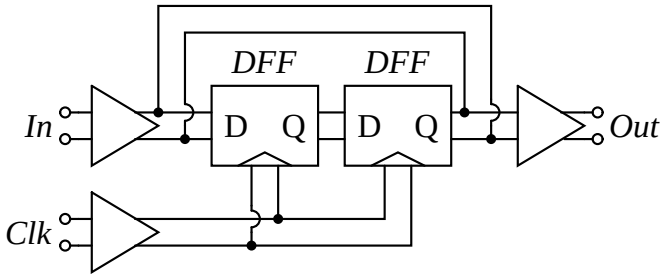
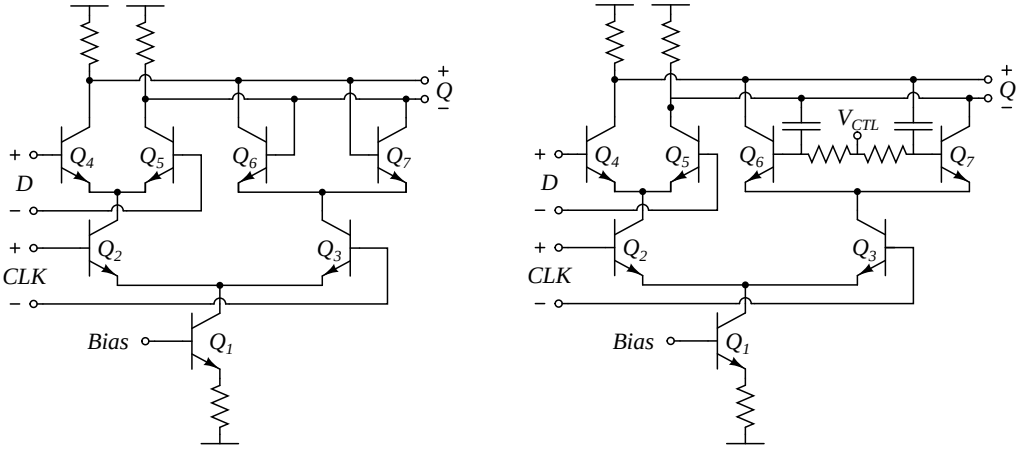


Figure 33: A block diagram of the digital frequency divider.

are implemented using CML gates as shown in Figure 34a. This architecture uses the clock signal to steer current between the differential pair sensing stage and the cross-coupled storage stage. Unlike CMOS logic levels that occur at the upper and lower voltage rails, CML logic levels occur at the upper rail voltage when no current is present or at a small voltage deviation from the upper rail voltage when current is flowing. These voltage swings are typically small, about 400 mV, which contributes to the high operation speed. The edge-triggered latch formed from cascading the D flip-flops together can have its output inverted and fed back to its input to form a simple divide-by-2 circuit. Since the CML topology is differential, the inversion from output to input is achieved by swapping the positive and negative terminals, as is the inversion of the clock signal.

Several theoretical analyses of residual phase noise in digital frequency dividers have been presented in the literature [23, 58]. Noise in these circuits will be defined as variations in the edge-triggered switching times of the D latch. Since this switching action is controlled by changes in the clock signal, the critical transistors for noise performance are the differential clock pair formed by Q_2 and Q_3 in Figure 34a. Although noise is dominated by clock switching, the load resistors and tail current generator will also contribute to the overall phase noise. In [58], the authors derive an expression for the noise floor at large offsets, which identifies the largest contributors in the term



(a) Standard D-Latch (b) Modified D-Latch

Figure 34: Current-mode logic D flip-flop schematics. (a) represents a standard circuit, while (b) represents the modified circuit presented here to improve phase noise.

$$\mathscr{L}_W \propto \frac{kTC_L}{I_B^2} f_{out}. \tag{78}$$

Although the theory is specifically centered around source-coupled logic using FETs, the major design implications from (78) will be identical for HBTs. The trade-off between bias current and phase noise is clearly the strongest relationship in this equation, since it has a quadratic dependence. Techniques to reduce load capacitance can also be beneficial, provided the buffers used do not contribute more residual phase noise than the benefit provided by the reduced load capacitance. Finally, the phase noise will be proportional to both temperature and output frequency, which should be noted when forming a figure-of-merit for comparisons of different frequency dividers.

Given this abstract understanding of noise in digital frequency dividers, the optimization process begins by selecting a technology platform. This design has used IBM's 8HP 0.13 µm silicon-germanium (SiGe) BiCMOS process. This technology contains IBM's third-generation SiGe HBT, with a peak f_T of 200 GHz and a peak f_{max} of 285 GHz. By using the fastest available SiGe HBT technology at the time, the dominant load capacitance formed by C_π of the D flip-flop input stages as well as

the output buffer is reduced and minimizes clock-edge jitter and therefor phase noise. The next step is to maximize current draw to reduce phase noise according to (78). Here, current is not limited by the current handling capabilities of the SiGe HBTs, but rather by that of the load resistors and the maximum output voltage swing. The output voltage swing of the divider will be defined by the voltage drop across the load resistors. As the current increases, the load resistance can be decreased to maintain a constant voltage swing. However, as the resistance value gets much smaller than the sheet resistance, the resistor width increases dramatically and the area requirements of the resistors become a concern. The IBM SiGe process offers BEOL thin film resistors that offer excellent RF performance and lower noise than integrated resistors using bulk-Si. They also have superior current handling capability and a low sheet resistance compatible with the goal of achieving low phase noise performance through increased current. The resistors were sized at the minimum width necessary to handle the current being drawn, and the length was assigned to be slightly less than one square in order to minimize area and maximize reliability.

With this lower bound restriction on resistor size, maximum current flow becomes limited by the voltage swing, which will be proportional to the current once the load resistance is fixed. In this regard, Figure 34a shows that the flip-flops are limited primarily by the sense and storage stages being driven into saturation. As the voltage swing becomes larger, Q_4-Q_7 will lose sufficient voltage headroom and begin to add significant noise to the divider that was not present when under forward-active bias. Because of the setup time requirement for proper latch operation, the saturation region of the sense stage occurs outside the clock switching time, and hence doesn't contribute significantly to divider noise [58]. However, the storage cell drive saturation occurs during the critical clock switching period. This is where a simple, yet novel circuit technique has been applied as shown in Figure 34b. By biasing the base of the storage cells separately, the collector-base voltage on these devices can be increased

and push the current higher before saturation limits the performance. This effect performs a similar function as the emitter-follower stage in buffered circuits without adding the additional noise through the buffer device.

The effect is best analyzed by looking at limit cycles, as illustrated in Figure 35. Here, the output voltage-current characteristics of the storage cell devices, Q_6 and Q_7, during steady-state operation at a 10 GHz input frequency. The blue trace denotes the operation of the standard design. The standard design forms a loop near the knee voltage area that defines the saturation resgion of the HBT. This section of the limit cycle occurs just as the device starts pulling current and injects excess noise into the output, since it occurs while the clock signal is switching. By contrast, the green and red curves show the new design with the base biased separately. The green curve represents a V_{ctl} bias point of 2.75 V on a 3.3 V rail, while the red curve pushes the bias point down even farther to 2.5 V. This demonstrates the concept that shifting this extra bias line from the top rail pulls the limit cycle of the storage devices away from the noisier saturation region and provides a cleaner signal during the clock transition periods.

Separating the bias of the storage cell in the manner shown in Figure 34b essentially introduces a high-pass filter into the storage cell of the D latch. Because it is difficult to make large capacitors on die, this filter may have a non-trivial corner frequency depending on the application. Frequencies below this corner frequency will show decreased sensitivity and eventually stop functioning. This can be problematic for synthesizers that operate across a wide band of frequencies requiring both low and high frequency inputs.

Early phase noise measurements of the frequency dividers relied on the use of baluns to transform the differential signal on die to the single-ended signal necessary to communicate with the measurement equipment. It was believed that this transformation would provide a phase noise improvement by offering a degree of

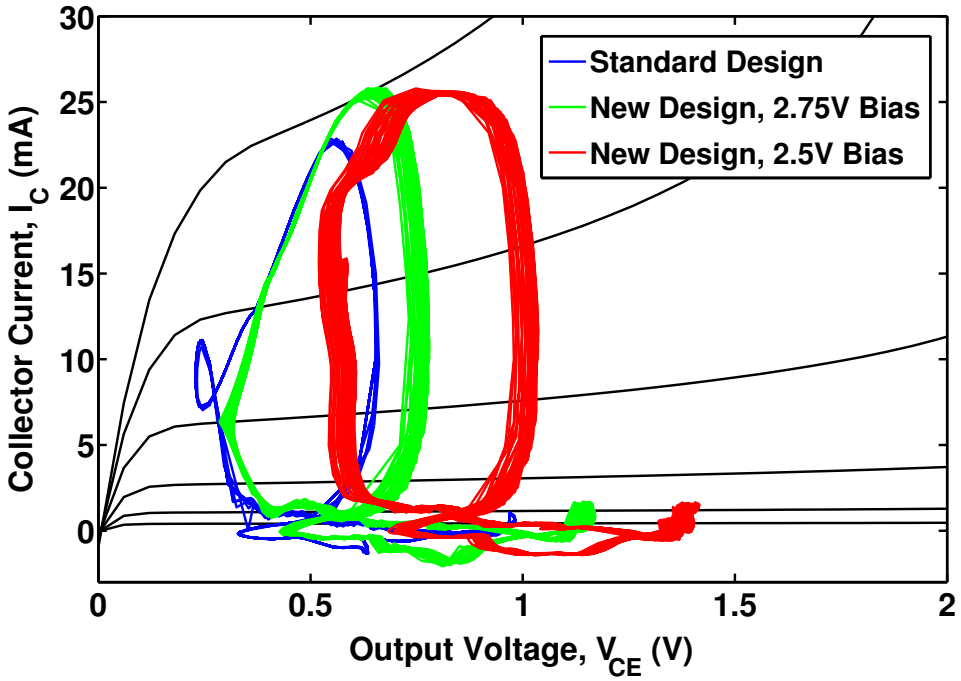


Figure 35: Limit cycle output characteristics of the storage cell. The blue trace indicates the standard design topology, while the green and red traces represent the modified design at biases of 2.75 V and 2.5 V respectively. The effect of this bias is to pull the limit cycle away from the strong saturation region of the device.

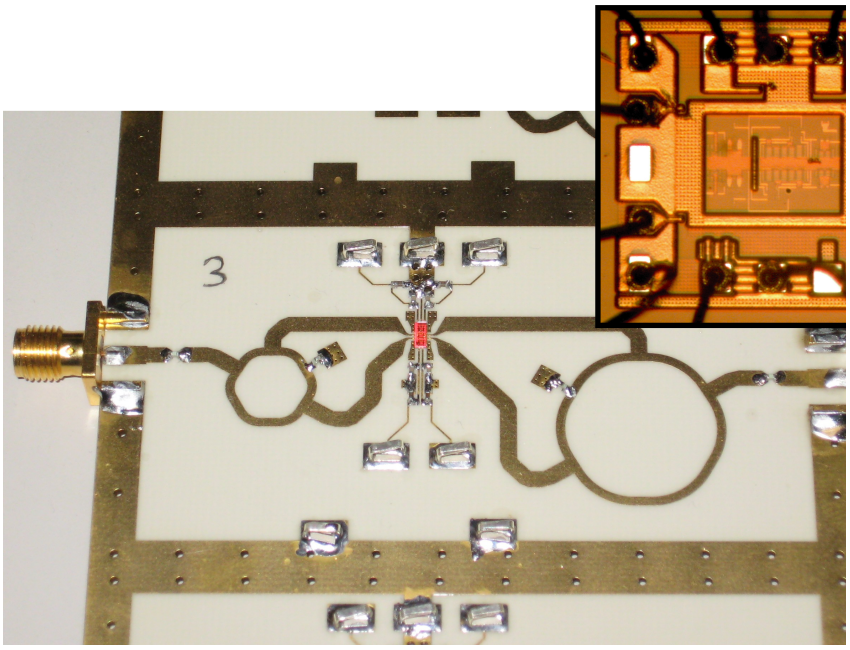


Figure 36: Photo of the frequency divider and their packages with rat race couplers used as baluns. The die is highlighted in red on the package. The inset shows a microscope photograph of the die.

common-mode noise rejection that would be lost by simply terminating one end into 50 Ω. Rather than using a cable-level balun, which would require the use of carefully phase-matched cables, baluns were built into the package. The package was fabricated using a Rogers high-frequency substrate. Rat race couplers were designed at 10 GHz for the input and 5 GHz for the output with the differential traces carefully phase-matched and hence much more accurate than cables. The custom package solution also enabled very large decoupling capacitance to be placed very close to the chip. Package and die photographs can be seen in Figure 36. Calibration structures showed that the insertion loss of the input section was 6 dB and the insertion loss of the output section was 5 dB. Thus, the loss of the baluns themselves proved a bigger obstacle to high dynamic range phase noise measurements than common-mode noise.

Residual phase noise was measured using the front-end configuration of Figure 20 on the phase noise measurement system. Two identical packages were built for each design: a control design using the standard D latch topology and a design using

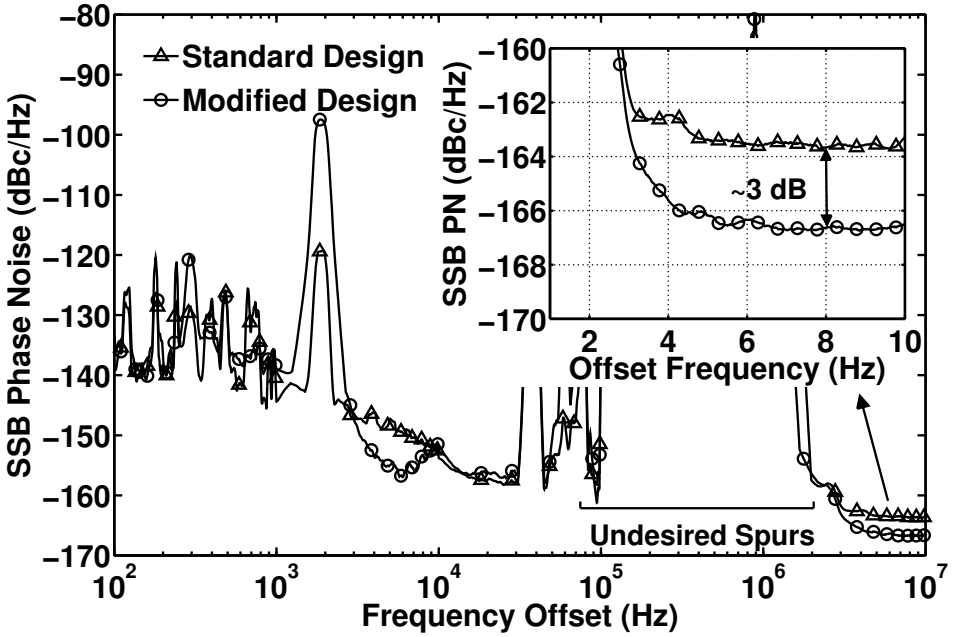
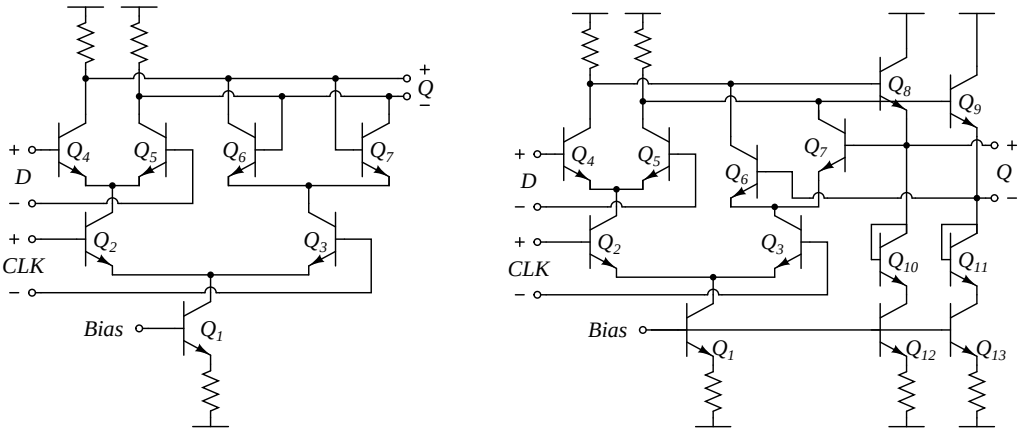


Figure 37: Measured SSB phase noise of the frequency dividers. Despite the presence of undesired noise spurs in the measurement, the effect on the residual noise floor is still clearly visible.

the separated bias for the storage cell. Both designs were identical with regard to transistor and resistor sizing, as well as current bias. The measurement results are shown in Figure 37. There were several regions of undesired spurs appearing in this measurement that masked the true phase noise response and make the results difficult to spot. There were a number of factors contributing to this limitation including poor bias line filtering and lack of a Faraday cage available to shield the measurement setup from the noisy background environment. Despite these limitations, the measurements can still validate proof of the concept. The residual phase noise floor of the control design and the package can clearly be approximated at around -163.5 dBc/Hz, while the new design shows a noise floor of approximately -166.5 dBc/Hz. This represents an improvement of around 3 dB. These results clearly indicate that adding an external bias to the D flip-flop storage cells can be used to decrease the residual phase noise in digital frequency dividers.



(a) CML D flip-flop (b) ECL D flip-flop

Figure 38: Current-mode logic D flip-flop schematics. (a) represents a standard circuit, while (b) represents the modified circuit presented here to improve phase noise.

3.2.2 Revised Frequency Divider Designs

The frequency limitations introduced by the modified flip-flop design of Figure 34b are potentially serious design limitations for frequency synthesizers with wide tuning ranges. Therefore, a follow-up study to the modified latch was conducted using emitter-coupled logic (ECL) gates. ECL is characterized by emitter-follower output buffers isolating the feedback of the cross-coupled storage cell of Q_6 and Q_7 as shown in Figure 38b. This technique is used to increase the speed of the latch and has been used to produce digital frequency dividers that operate up to millimeter-wave frequencies [54]. For the purposes of residual phase noise, adding the output buffer performs a similar function to the separated bias circuit of Figure 34b, but without the drawback of having a high-pass response. When fed back as in Figure 32, the DC voltage shift of the output buffers also keeps the amplifier stage of Q_1 and Q_2 out of saturation unlike the previous modified flip-flop design. However, the extra base-emitter potential required to keep the circuit biased introduces added strain on the rail voltage headroom, which becomes difficult to maintain at 3.3V.

In addition to the changes in comparison circuitry, changes were also made to

improve the layout of the first design. Since these circuits are intended to draw a large amount of current in order to minimize residual phase noise, self-heating becomes an issue. Reliability layouts provided in the IBM design kit as well as increased transistor spacing helped reduce fluctuation in measurements over time. Additionally, limiting diodes were added to the input of the frequency divider to allow a larger RF input amplitude. By clipping the peak amplitude of the sinusoidal input, the large voltage swings will not damage the devices, but the sharper transitions will help improve the phase noise.

The package for the second study has also changed significantly. Shown in Figure 39, the most notable difference is the removal of the rat race baluns. Differential inputs and outputs were preserved to attempt a measurement with wide bandwidth baluns from Picosecond Pulse Labs. However, these measurements produced the same results where loss in the baluns impacted the measurement more than the noise reduction they offered. Therefore, the packages were reconfigured for single-ended measurements to give the best results. Improved power supply filtering was also added to this package in the form of large decoupling capacitors close to the die in combination with a low noise linear voltage regulator. A glob material was also placed over the die to prevent accidental damage to the wirebonds.

The results of this follow up analysis are shown in Figure 40. The improvements made to this design, particularly for filtering the DC bias lines, have eliminated the large spurs that plagued the previous measurement. The data plotted shows the raw captured data after ten averages in gray, while smoothed data is overlaid as a solid line with markers. The dashed line shows the noise floor of the system with no DUT in place. The ECL frequency divider shows a similar 3 dB improvement over the CML frequency divider compared to the modified divider topology shown in Figure 37.

Without the fixed baluns on the package, it becomes possible to examine the frequency dividers across a broader range of frequencies. Figure 41 shows measurements

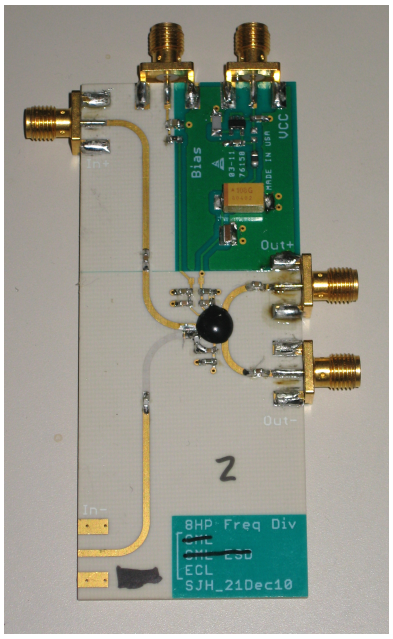


Figure 39: Photo of the revised frequency divider without baluns. These die are also encapsulated in glob top material for protection.

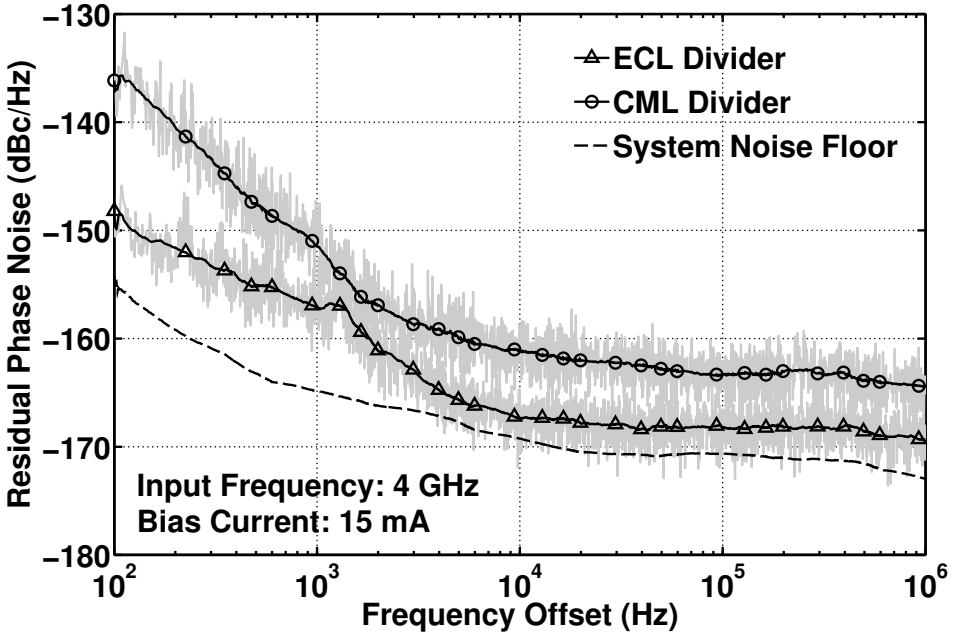


Figure 40: Residual phase noise measurements of ECL frequency dividers relative to an equivalent CML counterpart.

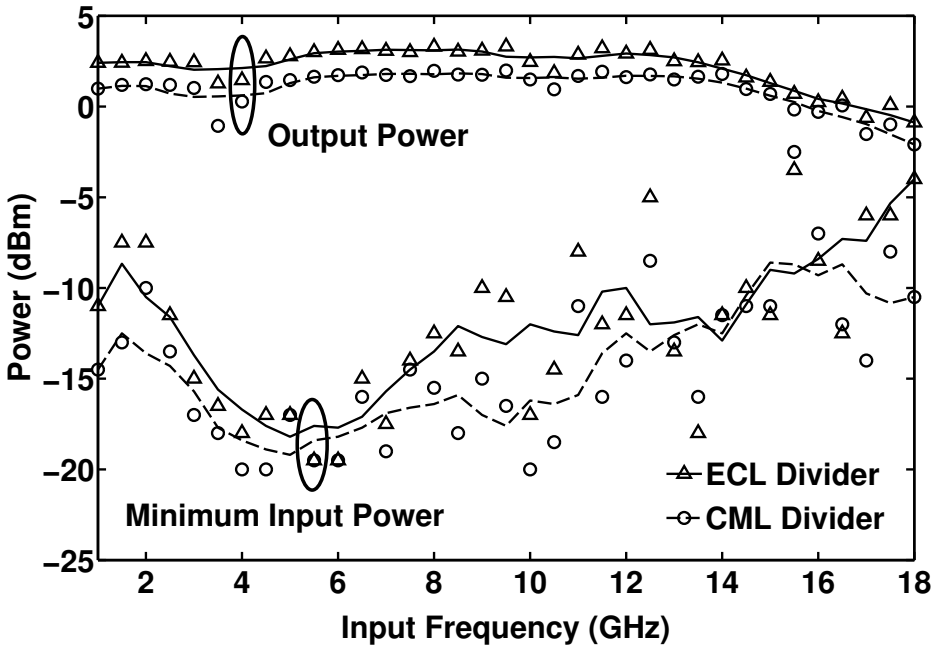


Figure 41: Minimum input power and measured output power across frequency. The solid line connecting data points is smoothed to reveal trends in the data.

of the output power as well as the minimum input power required for proper operation for input frequencies ranging from 1 GHz to 18 GHz. The trends revealed here highlight the reason why both the ECL and modified D flip-flop topology provide a phase noise advantage over standard CML frequency dividers. The feedback loop of the digital frequency divider from Q output to D input makes the output amplitude a function of the dynamics of the system. In both cases, the modified design and ECL design allow a larger voltage swing in the D latch than the standard CML design. These circuits accomplish this improvement by preventing the onset of saturation in the HBTs as the amplitude grows, allowing the steady-state amplitude swing to be larger than the control CML design. Since the noise sources of all of the circuits are held the same by design, the increased signal power directly improves the residual phase noise, a metric that captures the signal-to-noise ratio of the circuit.

3.2.3 Impact of the Designs

The proposed designs offer two methods of improving residual phase noise in digital frequency dividers. Beginning with established theory, frequency dividers improve their phase noise performance by reducing parasitic capacitance and increasing the bias current to the extent possible. The experimental designs then move beyond these considerations to improve the residual phase noise even further through enhancement of the signal swing. A first attempt utilized a separated pull-down bias in the storage cell to prevent saturation, while the second explored the use of an emitter-follower buffer that also shifts the bias point to produce the same effect. While there are particular instances where the separated bias circuit may preferable, particularly in low voltage rail situations, the ECL design is typically preferred. This is because the precise control required for the external bias in the modified design requires additional circuit overhead, and the introduction of bias separation introduces a high-pass filter in the design that limits the lower frequency operation.

As demonstrated in [58], the improved phase noise performance fundamentally comes at a significant cost in DC power dissipation. While operating on a 3.3 V rail, the CML design from the first study draws 115 mA, while the modified latch design draws 105 mA. This includes both the input and output buffers. Given the wide range of design constraints available, it is instructive to use a figure-of-merit (FoM) to normalize these trade-offs for comparison purposes and provide a benchmark for these results to those in previous literature. The following FoM is typically used to compare the phase noise of free running VCO designs and has similar application here

$$FoM = \mathscr{L}_{floor} - 20log(f_0) + 10log(P_{DC}) + 30 \tag{79}$$

The one change from the typical VCO figure-of-merit is that the term for the frequency offset has been removed since the noise floor is typically reported for frequency dividers and will be constant for large offsets. The FoM results of the present design

are compared with other frequency dividers in Table 3. These include a low phase noise part commercially available from Hittite. It should be noted that apart from the commercial product, this is the only design that was packaged during measurement.

Table 3: Comparison of frequency divider designs to recently published work.

Reference	Noise Floor	DC Power	Frequency	FoM
[54]	-90 dBc/Hz	122 mW	100 GHz	-289 dBc/Hz
[58]	-163 dBc/Hz	27 mW	78 MHz	-307 dBc/Hz
[1]	-150 dBc/Hz	375 mW	4.8 GHz	-318 dBc/Hz
[38] Standard CML	-163.6 dBc/Hz	380 mW	10 GHz	-337 dBc/Hz
[38] Modified CML	-166.7 dBc/Hz	350 mW	10 GHz	-341 dBc/Hz
[41] Second Design CML	-163.3 dBc/Hz	451 mW	4 GHz	-329 dBc/Hz
[41] Second Design ECL	-168.2 dBc/Hz	686 mW	4 GHz	-332 dBc/Hz

3.3 AM/PM Distortion in SiGe HBTs

Linearity often plays a limiting role in high dynamic range RF circuits using silicon-based semiconductor devices. Research efforts to improve linearity in SiGe HBT devices and circuits have typically focused on gain compression or intermodulation distortion; metrics that use a change in input amplitude to reveal changes in the output amplitude characteristics, or AM/AM nonlinearities [70]. An important parameter often overlooked in many applications is the phase deviation at large signal, so-called AM/PM nonlinearities. The concept of AM/PM distortion is not new, and first appeared in the development of communication systems theory [28, 84]. Recently, AM/PM nonlinearities have been analyzed in integrated varactor diodes used in resonant tanks to determine its effect on phase noise in oscillators [59]. A model to predict AM/PM distortion in HBTs using Volterra series was also recently presented, although to our knowledge no measured data was ever given to support their theory [44]. This section presents a new attempt to correllate AM/PM distortion in devices to relevant design considerations in voltage-controlled oscillators for frequency

synthesis. This begins with a preliminary characterization of AM/PM distortion in SiGe HBTs using traditional methods, first published in [37]. This is followed by an outline of a new technique using phase noise techniques similar to those developed in Chapter 2.

AM/PM distortion manifests itself as a change in phase with respect to the input power applied to the device. In an ideal linear system, the frequency domain phase response would remain constant across input power. A nonlinear signal, however, will introduce phase changes in the fundamental frequency similar to the spurious harmonics also generated. This is often overlooked because it is a critical concern only in certain types of electronic systems. The phase changes introduced as the device compresses are typically on the order of a few degrees, but even this small shift can have a significant impact on the operation of high data rate systems such as wireless LAN (WLAN). In the case of WLAN, the binary decision boundaries to interpret the 64 QAM constellation require very accurate amplitude and phase information be preserved in order to avoid bit error rate degradation. A phase error introduced by AM/PM distortion can lead to a significant increase in error vector magnitude (EVM), and in turn, bit error rate, degrading overall system performance. A similar process can influence the noise characteristics of oscillators [78]. However, although the theory predicts this influence, no measurement method exists to characterize the AM/PM distortion of device in a manner conducive to predicting phase noise performance.

3.3.1 Device Characterization

In order to observe the nonlinear phase deviation across all of the desired parameters, an integrated load-pull setup was used, which allowed for consistent calibrated measurements across various conditions. Shown in Figure 42, this Focus Microwaves system uses custom-built high-impedance probe tuners to tune the load to gammas of

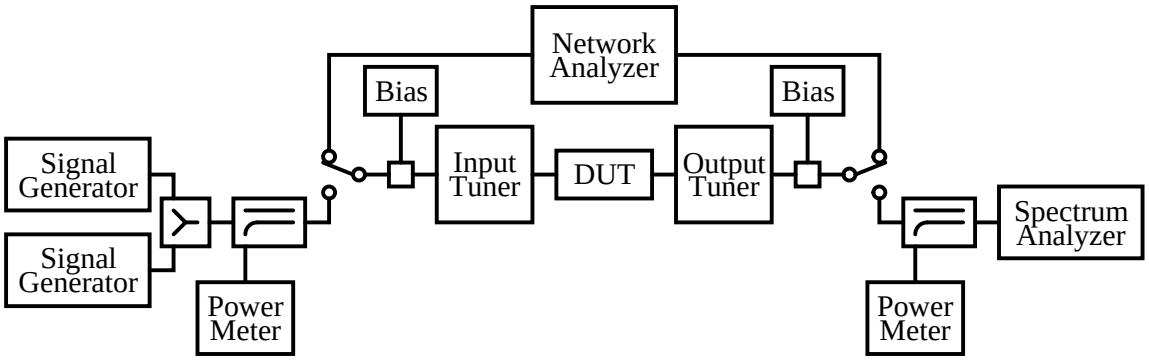
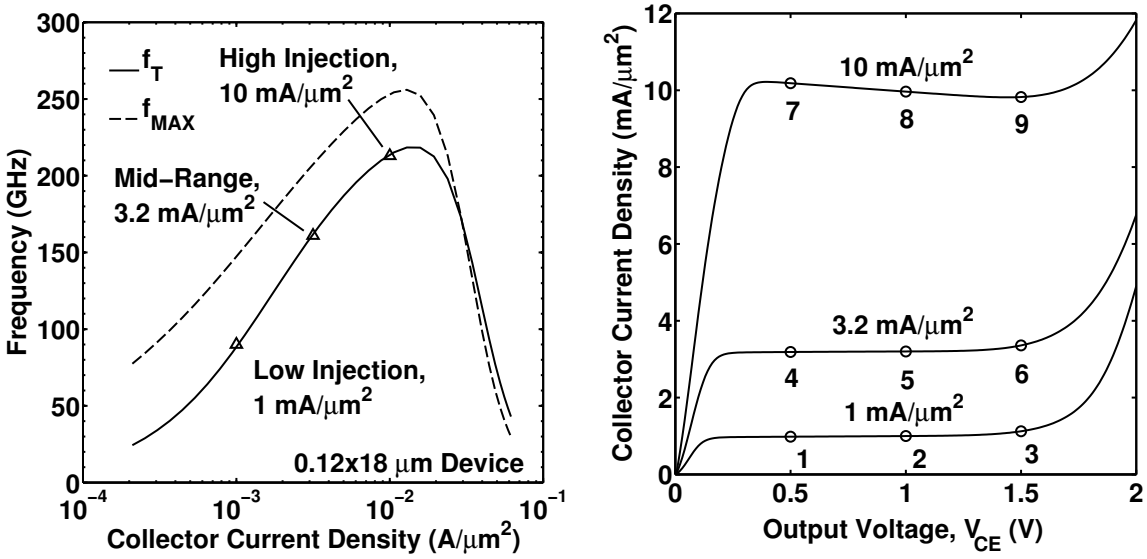


Figure 42: A block diagram of the network analyzer measurement setup for AM/PM distortion with source and load tuning capabilities.

up to 0.88. Once calibrated, a suite of measurements, including S-parameters, output power, gain compression, and third-order intercept point can be taken without ever lifting the microwave probes.

A static measurement was used to characterize the AM/PM distortion in a single decive, as outlined in [91]. This technique uses a network analyzer configured for gain compression measurements. Since AM/PM conversion is a phenomena that appears in the device during weakly nonlinear operation, it must be in compression to observe the effect. By measuring the change in phase of the calibrated insertion loss measurement as the device is driven into compression, the nonlinear phase deviation can be observed. An ideal device with no AM/PM conversion would show a flat phase response across input powers.

The test was conducted on IBM's 8HP platform, a popular commercial 130 nm SiGe BiCMOS platform. This technology features an f_T of 200 GHz and f_{MAX} of 285 GHz as seen in Figure 43a. A 0.12x18 µm SiGe HBT was measured, because it is the largest emitter size supported by the design kit and is a good representation of a geometry that could be found in a typical circuit where handling large signal conditions might be desirable, such as an oscillator or a power amplifier. A measurement frequency of 10 GHz was chosen because of load tuner limitations, but this approach can be easily translated to other frequency bands as needed.



(a) AC Characteristics

(b) Output Characteristics

Figure 43: Bias point selection for the preliminary study of AM/PM distortion. Maximum oscillation frequency, f_{MAX}, and unity gain frequency, f_T, are shown in (a). Output characteristics showing bias variation with V_{CB} are shown in (b). There are nine total bias points tested.

AM/PM distortion was measured across bias and load conditions across nine points spread across the forward active mode of the device. Figure 43 highlights the selection process for the bias points. First, points were chosen across collector current density based on the maximum current gain frequency, f_T, shown in Figure 43a. The three points chosen occur near the peak value, a mid-range value, and a low current density value that covers the range of typical HBT operation. Each of these points are also swept across collector-base voltage ranging from near saturation of the device to near breakdown. These points form a 3x3 matrix of bias points across the entire forward active region of the device as a means to observe the AM/PM performance of a SiGe HBT under a variety of typical conditions.

3.3.1.1 AM/PM Distortion Across Bias

An initial test was run to get a feel for the overall nonlinear phase performance of the SiGe HBT. Using the measurement setup described, the device was biased using both

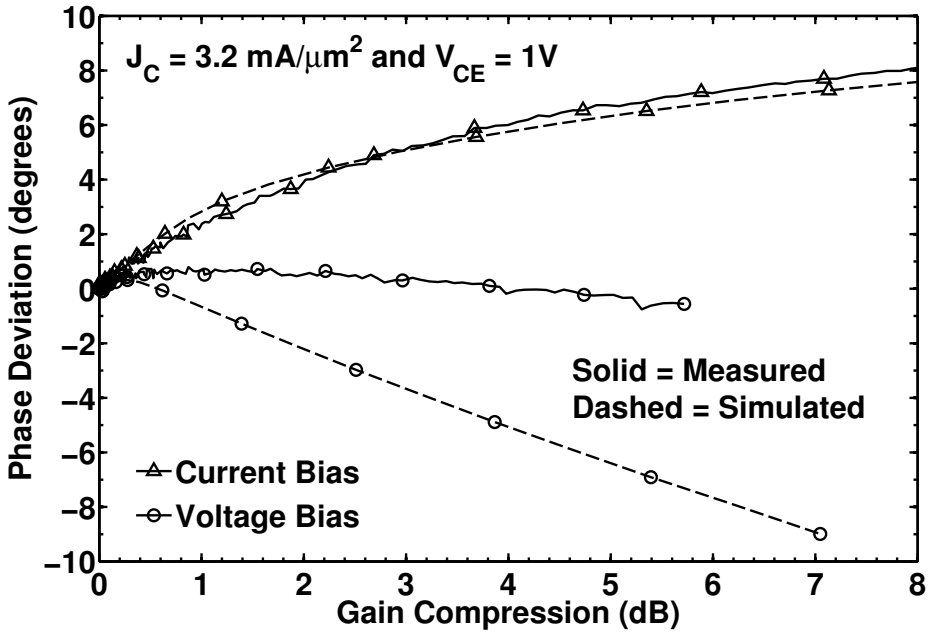


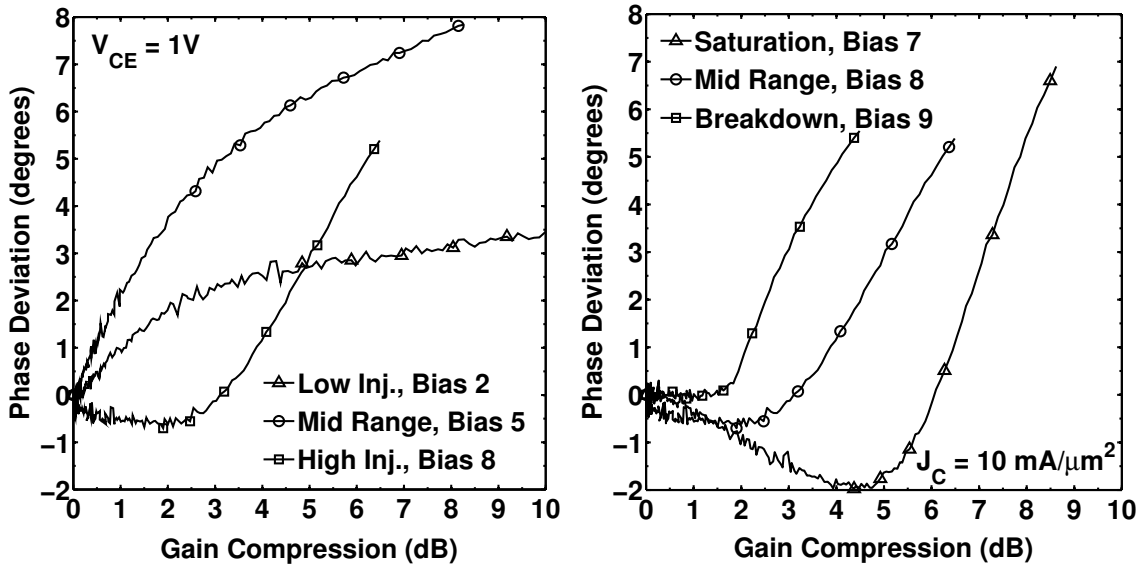
Figure 44: AM/PM conversion with forced voltage and current bias on the base. The solid line represents measurements, while the dashed line is a GoldenGate simulation based on a calibrated VBIC model.

a voltage source and a current source on the base-emitter junction. An equivalent simulation was run using GoldenGate, with the design kit provided VBIC SiGe HBT model. The results are shown in Figure 44 as phase deviation across gain compression. Recall that an ideal response should give zero phase deviation for any power level. Plotting this phase deviation over gain compression rather than the absolute power level is intended to give insight into phase distortion with respect to more familiar amplitude distortion metrics. In the current driven case in Figure 44, this implies that at a gain compression of 1 dB, when the input power is set to the P_{1dB} point, the phase will shift by slightly more than two degrees.

Figure 44 indicates that the VBIC model is reasonably accurate at predicting the phase deviation when the transistor is current biased, but not so accurate when a voltage bias is applied. The cause is self-biasing that cannot be captured using harmonic balance simulation techniques. As the signal level increases beyond the region where small-signal approximations are valid, non-linearities will generate frequency

components at multiples of the input frequency, including DC. This means a voltage signal will introduce a DC offset across the base-emitter input port under large signal conditions. If the input bias is a low impedance voltage source, this DC offset will superposition with the existing voltage potential across the junction to shift the bias point. If a high impedance current source is used, the DC offset will produce a potential change across the current source itself. As long as the current source remains constant under the voltage change, the bias point will remain the same. When simulating under voltage biased conditions, the large-signal S-parameter simulation uses a fixed DC bias point across the entire power sweep, and therefore cannot adapt to the changing bias occurring as the large signal input increases. The discrepancy in the bias point leads to the deviation from the measured data shown in Figure 44. In fact, the data suggests using an active voltage bias may potentially represent a way to mitigate AM/PM distortion, as the measured data shows almost no phase deviation well into gain compression. Note that a current bias cannot be used on the output terminal for a simple common-emitter test structure because that would leave V_{CE} floating, and changes on the input voltage would lead to output voltage changes that would cause the transistor to go constantly in and out of saturation.

Relevant data trends for AM/PM distortion are shown in Figure 45. Figure 45a shows AM/PM distortion varying across collector current. The low-injection condition corresponds to a collector current density of about 1.0 mA/μm^2, while the mid-range and high-injection conditions correspond to 3.2 mA/μm^2 and 10.0 mA/μm^2, respectively. The results demonstrate that as the device moves toward peak-f_T bias, not only does the gain compression decrease, as is evident by the shorter range on the x-axis, but the phase deviation actually flattens as the device goes into the early stages of compression. This 0-2 dB gain compression region is important because it represents the weakly nonlinear range, where gain compression will begin to limit positive feedback to produce a steady-state limit cycle.



(a) Collector Current Sweep (b) Collector-Base Voltage Sweep

Figure 45: AM/PM distortion measurements across bias. Variations in collector current are shown in (a). Variations in collector-base voltage are shown in (b). AM/PM distortion is minimized at high injection currents with the device near breakdown.

Using the information provided by Figure 45a, we next biased the device at the high-injection current density state and swept V_{CE} across three different voltages. This time 0.5 V, 1.0 V, and 1.5 V were used to bias the device near saturation, mid-range, and near breakdown, respectively, as shown in Figure 45b. The measured results indicate that although the phase deviation rises sharply after 2 dB of gain compression, biasing the device near breakdown effectively mitigates AM/PM distortion below that compression, which can be a very useful buffer zone to take advantage of in circuit design.

Using our optimal bias point of high-injection at near avalanche breakdown (BV_{CEO}), we then turned to simulations to observe how well the SiGe HBT VBIC model captures AM/PM distortion under this condition. The results in Figure 46 show that for the region of primary interest, from 0-2 dB gain compression, the simulation accurately models the data. This is good news for power amplifier design, since biasing in this region will give the largest output power. One cannot, however, overlook the

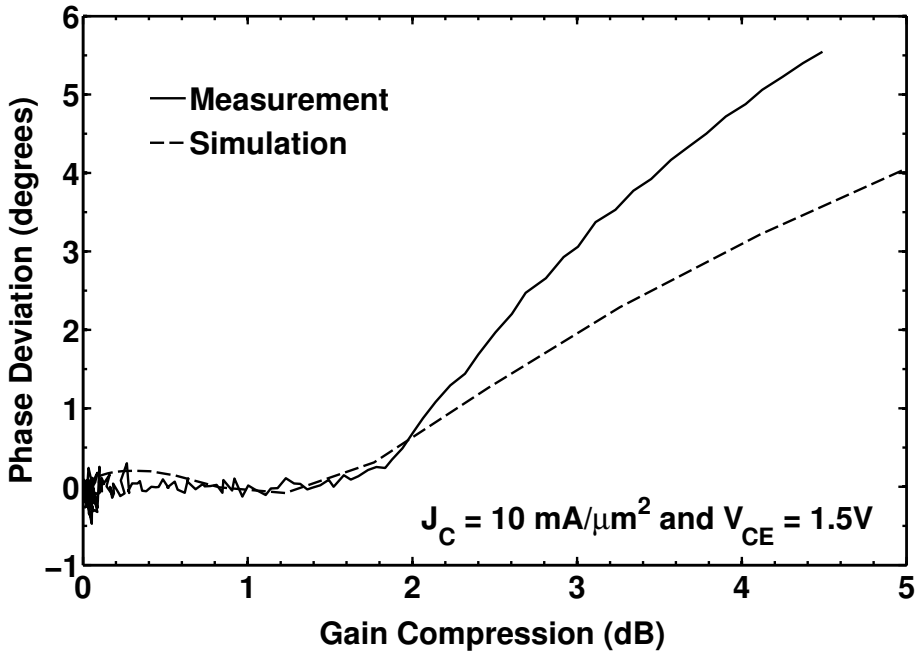
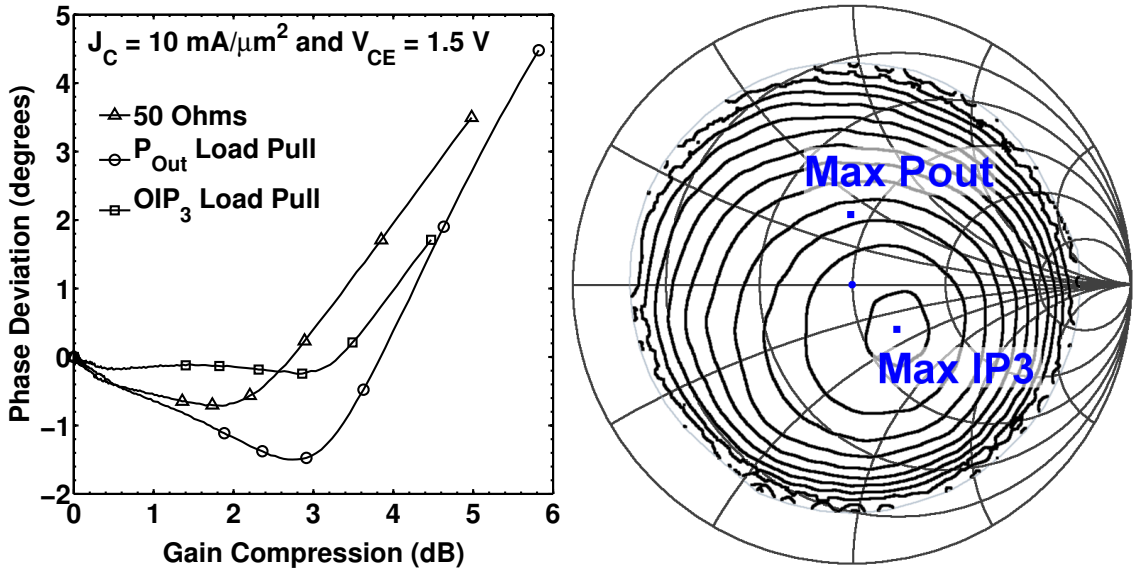


Figure 46: A comparison of measurements and simulations for the best case AM/PM conversion bias point at high-injection, near breakdown. The VBIC model captures the behavior very well at low gain compressions, where an amplifier is most likely to operate.

implications for the rest of the transceiver chain due to AM/PM distortion. Low noise amplifiers, buffers, and other devices that are typically biased at lower injection regions will also be susceptible to AM/PM distortion if driven toward compression. Receive chain low noise amplifiers, in particular, are often biased at low injection and can easily have a strong input signal send them into compression, thereby accentuating AM/PM distortion.

3.3.1.2 AM/PM Distortion Across Load

Since measurements across bias indicate that AM/PM conversion will have the least affect on devices biased for high output power, a logical follow-up question is whether a power match will enhance or degrade this effect. To test this, a load-pull measurement was run across various linearity parameters. The tuners were then set to these values, the switches were toggled to the network analyzer, and static phase deviation



(a) AM/PM Distortion over Load

(b) OIP_3 Load-Pull Contours

Figure 47: AM/PM distortion measurements for various load impedances. Matching to the peak output power load degrades AM/PM distortion relative to the 50Ω case, while matching to the maximum OIP_3 load seems to give the best response.

measurements across input power were taken, similar to the previous procedure. The results in Figure 47 show that a match to maximum output power similar to the procedure used to design power amplifiers in fact degrades the nonlinear phase deviation with respect to the 50Ω measurement.

Since matching to the maximum output power impedance degrades the AM/PM response, the next step is to determine what impedance provides the optimal match to minimize AM/PM conversion. We know that the effect derives from the nonlinear response of the device as the input power moves from small-signal to large-signal. Therefore, since we have no way of directly measuring the phase during the load-pull measurement, it makes sense to associate low AM/PM conversion with a corresponding AM/AM measurement. In this case, we chose to maximize the third order intercept point (IP_3). As seen in Figure 47a, a match to this impedance does in fact improve the AM/PM distortion by further flattening the distortion response to nearly zero degrees well into gain compression. The OIP_3 contours from the load

pull measurement can be observed in Figure 47b. The optimal match, which gives an OIP_3 of 16.9 dBm, is very close to 50 Ω. As a reference, the impedance for the maximum output power is also plotted in Figure 47b.

Based on devices measured from several different wafer lots, we theorize that the flattening effect initially observed at 50Ω is merely a byproduct of its proximity to the optimum linearity load point. Over a sample size of two transistors across three different wafer lots, devices whose maximum OIP_3 load point was closer to 50Ω generally showed improved phase flatness at 50Ω. AM/PM distortion at the optimum OIP_3 load deviated less than 1 degree from small signal at gain compressions of less than 2 dB for all samples. These observations seem to indicate that an optimum matching condition exists for AM/PM distortion that is closely tied to maximizing OIP_3. Since this load impedance differs from the maximum output power impedance typically used to design power amplifiers, a trade-off between linearity and output power seems applicable similar to the noise figure and gain trade-offs made in low noise amplifier design.

It is interesting to note that the optimum OIP_3 load point does not necessarily correspond to the maximum P_{1dB} load point. Measurements using this metric show the same trends as the maximum output power curves presented in Figure 47.

The results of this preliminary investigation show that the onset of AM/PM distortion can be pushed-out beyond the compression points of normal operation when biased at high-injection collector current densities. If AM/PM distortion is determined to be a limiting factor in a system of interest, these results suggest the following remedial procedures for integrated amplifier design:

- Ensure that each device in the critical path is biased in the high injection collector current density region. Moving the collector-base bias voltage close to breakdown will improve the results, while a move toward saturation will degrade them. Keep in mind that this would apply to any circuit operating in

the weakly nonlinear large signal regime, not just the power amplifier.

- Since AM/PM distortion seems to correlate well with inter-modulation distortion, tune the output load to the point that achieves the best OIP_3. If this load does not give sufficient output power, a trade-off between output power contours and OIP_3 contours can be made, using the collector-base bias voltage as a course tuning knob for the AM/PM suppression effect.

- If all else fails, changing the bias circuitry to use a weakly defined DC current by using only V_{BE} and V_{CE} also seems to provide some immunity to AM/PM distortion.

CHAPTER IV

RADIATION EFFECTS

The majority of electronic systems operate around a relatively narrow band of environmental conditions, similar to the range of environments a typical consumer might encounter on any particular day throughout the year. Critical electronics are held to more stringent standards in order to ensure reliability across a broader range of environments. These standards are primarily defined by military needs for operation in places such as jungles, deserts, and arctic theaters that are still hospitable to most life but otherwise outside the realm of the typical consumer. The United States military standards (MIL-SPEC) are frequently used as the design specifications for these applications. Extreme environments encompass circuits that must operate outside even these MIL-SPEC ranges. These can include cryogenic temperatures, high pressure or humidity, or the presence of ionizing radiation. This chapter will explore the impact of ionizing radiation on frequency synthesizer circuits, and the role SiGe technology can play to mitigate these effects.

Ionizing radiation is a phenomena at the atomic level where high energy particles, including photons, strip electrons from molecules in a target material. Ionizing radiation is prevalent in the solar system outside the protective magnetic field of the earth as well as the upper atmosphere. Collisions with these high energy particles are a considerable problem for space-based electronics, causing a host of maladies ranging from brief transient disturbances, to permanent circuit damage, to complete system failure [67]. A diagram of the Earth's magnetosphere is given in Figure 48. Satellites in low earth orbit encounter the trapped charge in the inner and outer Van Allen belts, dominated by protons and electrons respectively. These particles enter the

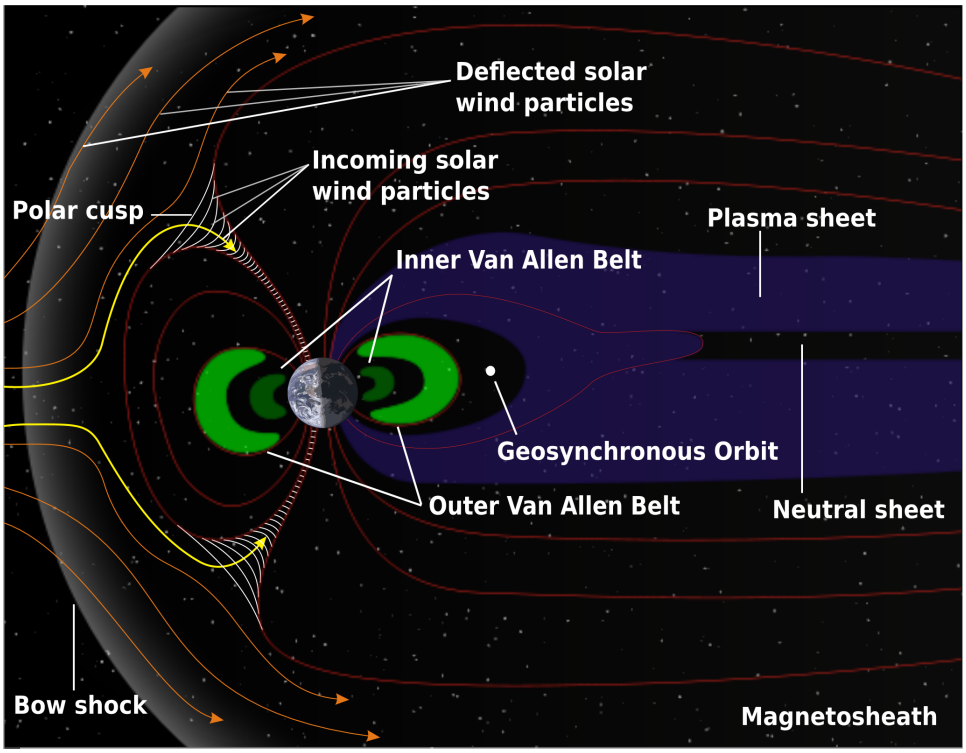


Figure 48: The Earth's magnetosphere highlighting dominant radiation sources.

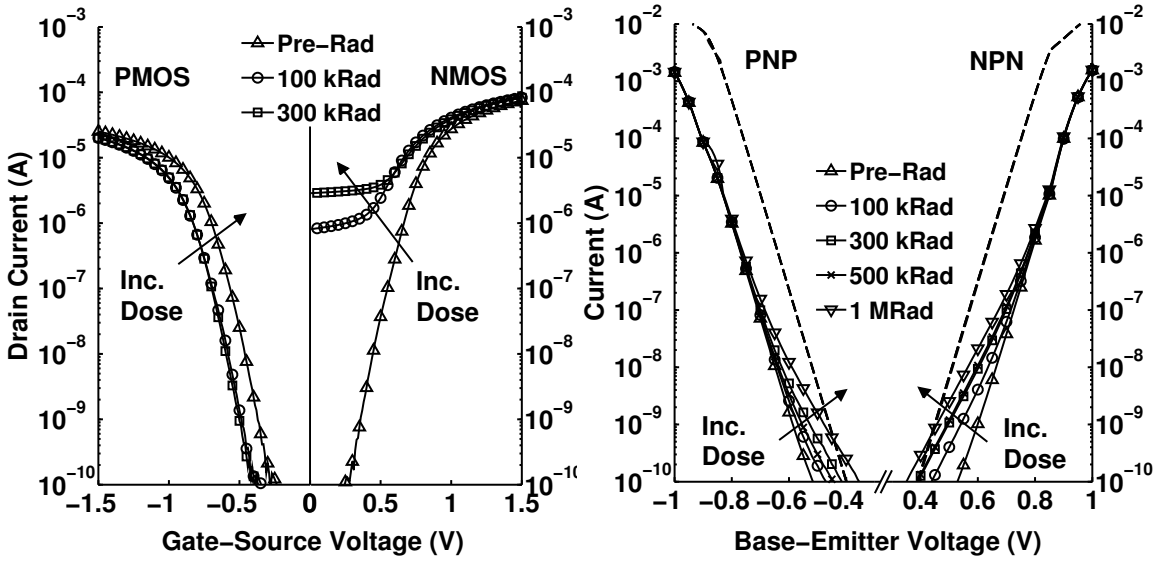
Earth's magnetic field through the polar cusp and become trapped inside it. Meanwhile, the plasma sheet contains hydrogen, helium, and oxygen particles ejected from the atmosphere. The remainder of the solar wind particles are deflected around the magnetosheath. Heavy ions traveling through interstellar space, the remnants of supernovae, as well as a small portion of the solar wind are also interspersed throughout the solar system but typically deflected by the Earth's magnetic field. The type and severity of impact on solid-state electronics is highly dependent on where the circuit operates relative to these radiation sources, and can be categorized into three broad groups: total-ionizing dose effects, displacement damage, and single-event effects.

Total-ionizing dose (TID) is a metric of the total energy absorbed by a circuit accumulated over time, traditionally given in Rad units. Since the energy absorbed is dependent on the material absorbing it, the dose must be referenced to that material. For integrated circuits, the absorbed energy is typically referenced to Si or SiO_2. The

impact of TID thus compounds over years of operation and limits the useful lifetime of the system. The mechanism for TID effects in semiconductor electronics are the production of trapped charge created by collisions with ionizing particles or photons. The silicon dioxide used as electrical isolation between transistors and interconnects is particularly susceptible to these effects. For MOSFET transistors, these effects manifest themselves as voltage threshold shifts. In processes that rely on shallow-trench oxides to provide isolation between the drain and source, the charge traps introduced by ionizing radiation also provide a leakage path for current between the drain and source. This situation is most typically found in n-channel devices, resulting in a loss of gate control for the devices in that a finite current continues to bleed from drain to source even when the gate is turned off.

SiGe HBTs respond to TID by an increase in base current leakage. However, these effects are significantly less drastic than those afflicting MOS devices. Figure 49 shows the forward transfer characteristics of devices in National Semiconductor's CBC-8 SiGe BiCMOS process. The MOS devices exhibit an off-state leakage of 2 µA when exposed to a TID of 300 kRad(Si), leaving only a single order of magnitude difference between "on" and "off" conditions. In contrast, the HBT devices are exposed to a TID up to 2 MRad(Si) [97]. Although these devices show base current degradation at low base-emitter voltages, the effect is small enough to leave many orders of magnitude in current conduction difference. For analog circuits and high speed logic that relies on differential pair switching, base-emitter voltages are maintained on the order of 0.7 to 1 V and therefore never even encounter these effects. For these reasons, circuits designed with bipolar transistors, such as SiGe HBTs, have a built-in immunity to TID effects. This immunity gives them an inherent advantage over the more ubiquitous MOSFET transistor [19].

Displacement damage is a completely separate effect from TID and is caused by the physical damage produced from particle collisions. Displacement damage includes



(a) MOSFET TID-Induced Leakage (b) HBT TID-Induced Leakage

Figure 49: Forward transfer characteristics for devices exposed to a total ionizing dose of gamma rays in the National CBC-8 SiGe BiCMOS process.

a variety of effects that can impact the electrical behavior of an integrated circuit. These can include damage to the crystalline-lattice structure that introduces vacancies and interstitial defects as well as dopant de-activation that makes subtle changes to finely tuned carrier concentration profiles. These effects are not considered in this work, but have been explored at the device level for SiGe BiCMOS platforms in [89].

Single-event effects (SEE) encompass the remainder of phenomena induced by ionizing radiation. These include the widest variety of effects and can have most serious consequences on circuit performance, but they are also the least likely to occur. Single-events are, as the name might imply, random occurrences caused by a collision of a high-energy charged ion with a sensitive location on a circuit producing an undesired electrical response. These effects can include single-event latch-up (SEL), which requires power cycling to return a digital circuit back to an operational condition, as well as single-event upset (SEU), which changes one or more bit states of digital logic cells. In analog circuits, single-events produce transients of varying magnitude known as single-event transients (SET). These effects are the most dominant SEE concerns

that will be addressed here.

The interaction causing SEEs stems from the charge produced from collisions with an individual ion. As the charged ion passes through a region of semiconductor material, it transfers its electric potential to the material creating electron-hole pairs as it goes. This leaves a track of free carriers in the vicinity of the path traveled by the ion. The way these carriers recombine or are swept into the circuit determines the phenomena observed. Understanding of these characteristics has led to a number of mitigation strategies, particularly for digital circuits. Additional spacing and substrate contacts in all digital logic cells can eliminate the conditions necessary to produce latch-up in CMOS circuits [25]. Likewise, triple-modular redundancy (TMR) is the traditional method for correcting SEU faults. This methodology reproduces the circuit three times and combines the result with a voting circuit. An SEU event creates an error in one circuit, while the other two give the correct result. Thus, the majority result overrides the erroneous SEU and the fault is suppressed. Although this method effectively suppresses SEU errors, it has the drawback of tripling the area and power requirements for a hardened circuit. Thus, research continues on methods to provide adequate radiation tolerance for digital circuits with reduced power and area overhead [49]. This chapter will address the most appropriate ways to deal with SETs in mixed signal frequency synthesizer circuits, which do not have the strong supporting framework for analysis that has been built-up around digital logic.

The built-in tolerance to TID suggests that the SiGe HBT has a significant role to play in a balanced approach to radiation hardening. Although SiGe HBTs are inherently immune to performance shifts from TID effects, they remain susceptible to SETs caused by a localized heavy ion strike [72]. The transient magnitudes in HBTs are shown to be significantly larger than those in MOS devices. The resulting trade-off between TID and SET performance implies careful design based on the mission-specific expected radiation environment is prudent. In terms of the larger

system, there is concern that SEEs can significantly affect the performance of a feedback control system like the phase-locked loop (PLL) used for frequency synthesis, especially if the event necessitates a re-acquisition of the locked state. The work presented here attempts to progress the state-of-the-art knowledge in identifying the analog-based transients at the output of the frequency synthesizer and the translation of these transients to useful bit error rate information that is critical to system designers.

4.1 Current Single-Event Metrics

The characterization of SEEs is a complex task because there are numerous factors that determine the quantity and location of energy deposition in the circuit, none of which are deterministic. Energy transfer from an ion strike at a given location will depend on properties of the ion such as mass, energy, and angle relative to the substrate as well as the ion's momentum as a function of penetration distance in the material. The accepted metric for quantifying energy transfer for engineering purposes is linear energy transfer (LET) expressed in MeV*cm^2/mg. This metric gives the rate of energy loss per unit density, which will not be constant as the ion penetrates into the substrate. Therefore, the convention is used to calculate LET at the substrate interface to produce a single number metric. This complex calculation is typically done using the Stopping and Range of Ions in Matter (SRIM) computer software package [100].

To gain a physical understanding of energy transfer during an ion strike, it is useful to consider relative scenarios. Figure 50 presents a relative understanding of LET for different heavy ions and energies available at the Lawrence Berkeley National Laboratory's 88" cyclotron. The figure is known as a Bragg curve and shows a heavy ion's LET as a function of the penetration depth in the material. For the two ions shown, the heavier Krypton ion clearly deposits more energy than the lighter Neon ion

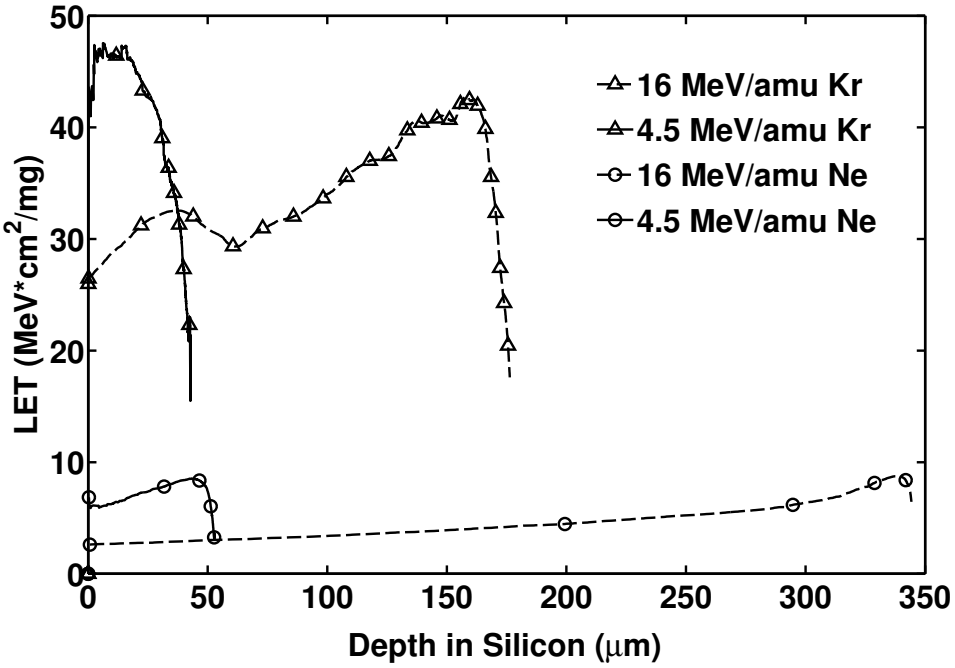


Figure 50: Bragg curves highlighting LET distribution for various heavy ions and energies.

and does not penetrate as deep into the substrate. However, note that higher energy ions transfer less energy at the silicon interface than lower energy ions of the same species. This can be intuitively understood as the ions colliding through the material with such speed that there is less time to transfer the energy to the material so the ion penetrates deeper but leaves a sparser charge track. At radiation facilities, circuits are tested with a variety of ions to generate statistical data at a number of different LET values. This parametric analysis is a tool that can be used to gather insight into the performance of the circuit for random single-events. The tool CREME96 can translate this data into predictive models for the number of errors expected in a given orbit [2, 93].

For digital circuits, the primary concern is preventing bit errors. A simple metric for SEU is thus the number of bit errors for a given number of ion strikes. This metric is the error cross section of a circuit and is defined as

$$\sigma_e = \frac{N_e}{\Phi}, \tag{80}$$

where N_e is the accumulated errors and Φ is the accumulated ion flux, or fluence, over a measurement period. The error cross section has units of area, cm^2. This effective area metric has the advantage that the location of ions striking the target do not need to be precisely controlled. Ions that strike outside the target area will not cause an error and thus not contribute to the effective sensitive area. The error cross-section metric is effective for digital circuits because errors have a known constant magnitude. A binary zero in error must be a one and vice versa. However, once this method is applied to analog signals, the error cross section fails to fully characterize an SET.

An ion strike in an analog circuit will produce a transient response at the output of the circuit. Unlike synchronous digital circuits, these analog transients will have magnitudes and durations that vary widely between individual strikes. If a critical threshold can be determined for the analog transient, the error cross section can still be used to determine an effective sensitive area. A separate metric is still needed to quantify the magnitude though. A few examples of analog transient characterization techniques exist in the literature [3,9,71]. However, these methods are not tailored to the specific needs of mixed-signal circuits in a phase-locked loop. A significant portion of this chapter is dedicated toward developing methods to understanding transients that best characterize PLL circuits, and presenting that information in a meaningful manner to system designers.

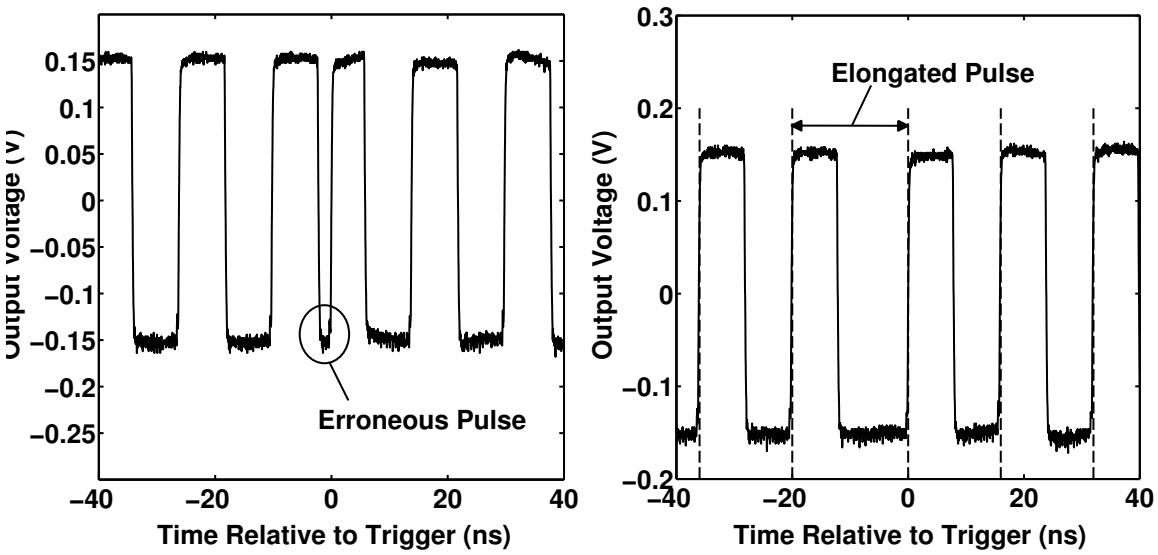
4.2 Characterization of Frequency Dividers

Digital frequency dividers are commonly used in modern frequency synthesis to provide precise control of the output frequency and comparison frequency at the phase detector. As demonstrated in Section 3.2, frequency dividers placed at the synthesizer output can also be used to further reduce the output phase noise of the closed-loop

synthesizer. One might expect that since these circuits produce a binary output, the standard metrics for SEU would be well-suited here. However, because the frequency divider sets the rate of a known alternating binary signal rather than pushing through unknown data bits at a known rate, the critical metrics for this block will involve changes to the frequency rate at the output of the circuit. These changes will not necessarily be discrete and thus must be treated in a more analog sense. The impact of these errors on synthesizer performance has been studied in [63]. This section briefly explores attempts to apply tested mitigation techniques to digital frequency dividers and provide a standard example of digital SEU metrics to contrast with the development of new methods in the following sections.

The impact of SEU on a digital storage cell is typically characterized using shift registers. These circuits cascade long chains of identical latches to gather statistical insight on the sensitivity of the latch. The SEU impact on an arbitrary system can then be estimated by the number of latches contained within the system. Several techniques have been published to reduce the error cross-section of a latch without resorting to a fully TMR method that would triple power and area requirements [49, 69, 90]. Many of these methods include changes to the latch architecture. We chose to translate the gated-feedback cell (GFC), a particularly promising architecture for shift registers outlined in [49], to a frequency divider configuration for analysis of SEU mitigation. Translating a shift register to a frequency divider in this case simply involves feeding the Q output of the latch back to the D input. This unstable feedback translates data errors into rate errors. Thus, the impact of SEU on the divider configuration cannot be assumed from shift register measurements.

Measurements comparing the GFC latch architecture to a standard CML architecture were conducted at the Texas A&M Cyclotron Institute. A variety of ion species were accelerated to 15 MeV/amu producing a range of effective LET values used to generate an error cross-section curve. Two forms of transients were observed in these



(a) Erroneous Pulse Error (b) Elongated Pulse Error

Figure 51: Two transient classifications observed during frequency divider measurements.

latches. Figure 51a shows an erroneous pulse where the strike produces a brief change in state not associated with a clock edge before returning to the nominal state. This type of transient produces the largest errors because the edge-detection circuitry of the phase-frequency detector will interpret this change as a significant variation in the output frequency of the divider. Figure 51b shows an alternative transient classification where the existing period of oscillation is merely elongated from its original for one period, producing much smaller variations in frequency. The impact of these variations on the output of the frequency synthesizer will depend in large part on the dynamics of the closed-loop system. A narrow loop bandwidth PLL might not show any influence from the strike because the long time constant around the loop reduces the influence of a single-cycle deviation, while a wide loop bandwidth may disturb the phase of the steady-state output waveform.

Figure 52 shows the error cross-section of the two designs. In this instance, an error was defined as any event that causes the frequency of the divider to deviate more than a minimum threshold. This measurement was accomplished using an

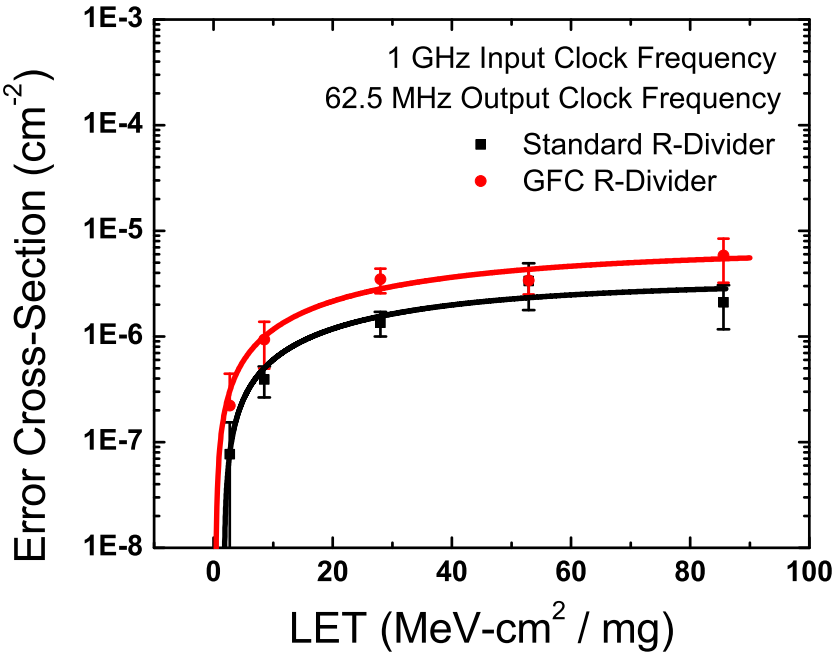


Figure 52: Comparison of error cross-section for frequency dividers composed of GFC and CML latch architectures.

oscilloscope with a width trigger and FastFrame technology for rapid re-arming of the trigger. The number of trigger events captured by the scope was divided by the fluence of the cyclotron to give the error cross-section. Note that the GFC design has a consistently higher cross-section than the standard CML design across the entire range of LET. A larger cross-section conveys that the likelihood of an error occurring is greater in the GFC latch than it is for the CML latch; an undesirable result since the GFC latch was intended to mitigate errors.

Despite the rise in error probability in frequency dividers, the GFC cell has been demonstrated to reduce errors in shift registers [49]. The most likely cause of this discrepancy is that the output is much more sensitive to excess charge in the feedback configuration of a divider. CML latches without feedback will give an incorrect state when a strike occurs temporally near the clock edge of a latching event. When the latch is in the feedback configuration, it is possible that the conditions needed to

change the latch's state is no longer a necessary condition for error in the frequency divider. For example, a flipped bit in the latch will still cause an error in the frequency divider, but so will smaller charge-induced transients that do not occur at the correct instant. We hypothesize that the observable classifications of transients in these dividers can be tied back to the event that caused them. For example, an erroneous pulse might be caused by a critical bit flip event, while an elongated pulse might be caused by a sub-critical charge-induced event. This hypothesis is currently in the process of being tested with a dedicated experiment to confirm the observed results.

4.3 Characterization of Charge Pumps

In modern integrated frequency synthesizers, the charge pump is used to . sub-block has been identified as a critically sensitive circuit in this regard. In [12], simulated transient injections in the charge pump produced the most significant system level disturbances. The work of [60] and [99] sought to mitigate these single event effects through design changes in the charge pump circuit. Recently, a linearized model describing the closed loop response of a PLL to a single-event ion strike has been described; clearly identifying the role of charge pump transients in the larger system scheme [62].

In addition to single-event effects, charge pump circuits may also be influenced by the total-ionizing dose (TID) accumulated over their time spent in space. This phenomena is distinct from single-event effects and produces gradual and permanent changes in the voltage-current relationships of the MOSFETs that comprise typical charge pump circuits. MOSFETs that lie outside a well, such as an n-channel device in an n-well only process are particularly sensitive to TID. Here, the accumulating ionizing radiation produces trapped charge in the shallow-trench oxide (STI) surrounding the active area of the device, allowing current to bypass the semiconductor channel controlled by the gate voltage [64]. These effects are potentially harmful for

circuits that rely on precision current values, which includes the charge pump.

This section investigates the impact of TID mitigation strategies on charge pump circuits. Two design philosophies for mitigation of TID degradation are explored. The resulting impact on single-event transients are also given, enabling a complete understanding of design trade-offs. The analysis combines measured observations with circuit modeling and simulation to present a comprehensive picture.

4.3.1 Charge Pump Design Strategy

Figure 53 shows a typical charge pump implementation for an integrated PLL. Two current sources with opposite polarity are attached to the control node, CPOUT, through their respective switches. If the phase of the VCO leads the reference, the charge pump decrement switch turns on for a time proportional to the phase difference, sinking current by pulling charge off of the loop filter capacitor. This action lowers the voltage on the control node and in turn reduces the VCO oscillation frequency to bring the phase into alignment with the reference. Similarly, if the phase of the VCO lags the reference, the increment switch turns on sourcing current, thus putting charge onto the loop filter capacitor. The alternative path for the current when these switches are off maintains the voltage headroom across the current sources, which allow them to stay on for fast operation. The op amp furthers this by mirroring the voltage on the output node to the dummy node, reducing charge-sharing effects brought on by voltage differentials across parasitic capacitances that produce switching spurs at the output. Charge pump circuits such as these are typically implemented using MOSFETs for several reasons. MOS devices, unlike BJTs or HBTs, can be used as the digital switches shown in Figure 53. In addition, reduced headroom requirements to keep the MOS device operating in saturation allows cascoded devices that produce superior output resistance while still allowing the control voltage on the output node to swing within 0.5 V of either supply rail. High output resistance is

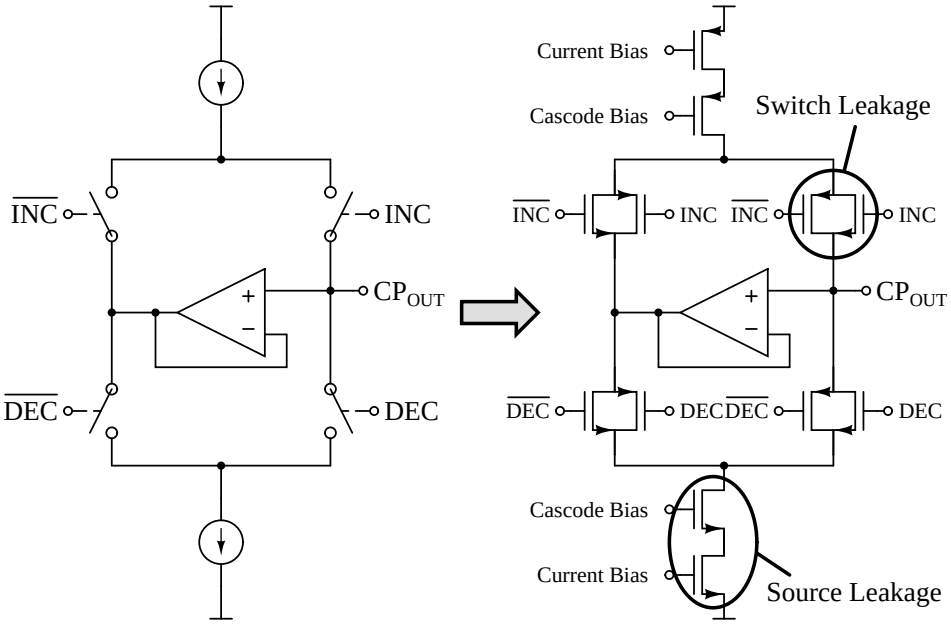


Figure 53: A schematic representation of a typical charge pump circuit for PLL applications. There are two areas of potential concern given off-state leakage observed in standard n-channel MOSFET devices.

important because it maintains a more constant current with variations in control voltage.

There are two potential problems with the typical implementation when dealing with leakage induced by TID radiation. The first problem lies with the switches. In a locked condition, the charge pump should be in a tri-state condition where both switches are off with a high degree of isolation preventing excess charge from entering or escaping the loop filter capacitor. Radiation-induced leakage will reduce the isolation of the switches and hence allow charge to constantly flow on the loop filter, in turn requiring constant adjustment by the charge pump to maintain a locked state. In addition, because most MOS platforms use an n-well process flow, n-channel devices suffer leakage through the STI while p-channel devices do not. Since the current sources are composed of complementary devices, a current mismatch between sinking and sourcing current sources is expected after prolonged exposure to radiation. Both of these effects produce spurs in the closed-loop phase noise response of the

PLL [7]. The introduction of these spurs directly contributes to the front end bit error rate in a frequency synthesis application [68].

Two different design approaches have been taken here as potential mitigation solutions to the problem of radiation-induced leakage in the charge pump. The first approach uses annular/enclosed gate layouts (EGL) for the sensitive n-channel devices. The change in device layout is highlighted in Figure 54. The polysilicon gate completely encloses the drain, eliminating the STI overlap between source and drain that introduces leakage using the standard gate-stripe layout. This technique is frequently used for digital circuits, but has not been applied to an analog circuit, to our knowledge. The design approach taken here is to perform a direct substitution of traditional gate-stripe structures with annular structures based on a calculation of equivalent W/L ratios [4]. The resulting circuit can therefore maintain an identical circuit to the standard design, at least to first order. There are, however, several drawbacks to this approach. The EGL is less compact than traditional layouts and thus consumes more die area, which results in nearly a 1.5x penalty. The biggest concern, however, is that these EGL devices are not modeled within the design kits. Although the W/L ratio is roughly equivalent, parasitic capacitances will be significantly different, and only a first order hand calculation of these parasitics is available [31].

The second mitigation approach taken here is to completely replace the n-channel MOSFETs with SiGe HBTs. A comparison of off-state leakage between the two devices on the National Semiconductor CBC-8 platform used for this study shows the traditional result. Although the HBT exhibits some base current leakage, it occurs at low injection levels below the typical operating region of the HBT and thus produces negligible impact on performance [15]. However, the charge pump requires a new paradigm of operation to use the HBT exclusively, because the switching speed using the architecture of Figure 53 is significantly degraded when the bipolar device is pushed into saturation. Our solution here has been to use the current steering

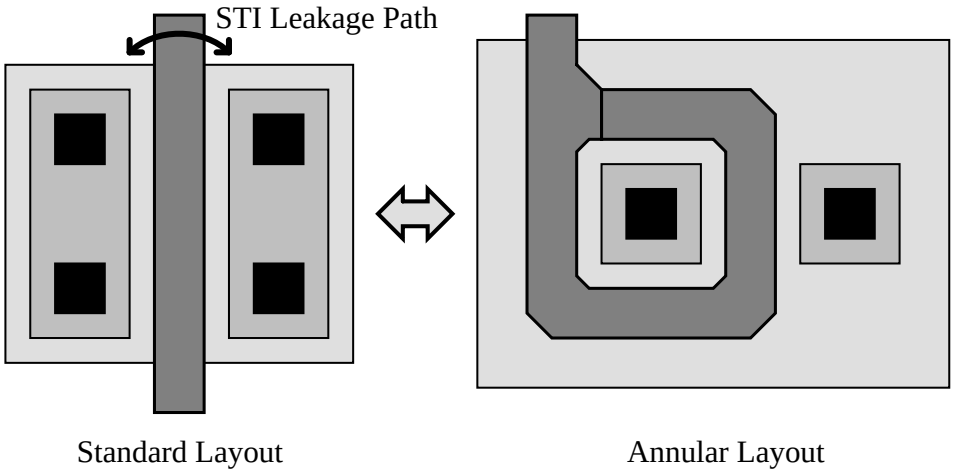


Figure 54: Comparison of standard and annular MOSFET layouts. By enclosing the drain region with the gate, the STI leakage path causing concern for charge pump circuit performance is cut off.

scheme shown in Figure 55. This approach is similar to high speed current mode logic (CML) that keeps the HBT in the forward active region by steering currents between differential branches. When the differential switch is turned on, the current is mirrored to a push-pull output stage where it can source or sink current and still allow the output voltage to swing within 0.5V of either rail. Operation of this circuit at high comparison frequencies is made possible by the use of a matched-performance vertical SiGe pnp HBTs in the CBC-8 process [5]. This C-SiGe design takes significantly less die area than the traditional design since the dummy stage and op-amp required to maintain voltage conditions are no longer necessary, and the HBTs are fully modeled in the design kit from the start. The drawbacks to this design are that the power consumption is increased because current through the differential switches is always flowing, and the output resistance is decreased because the HBTs do not provide enough headroom for a cascode configuration.

4.3.2 Total Dose Performance

The three charge pump variants were exposed to gamma radiation in a Cobalt-60 cell at National Semiconductor at a dose rate of 142 rad(Si)/s. The parts were each

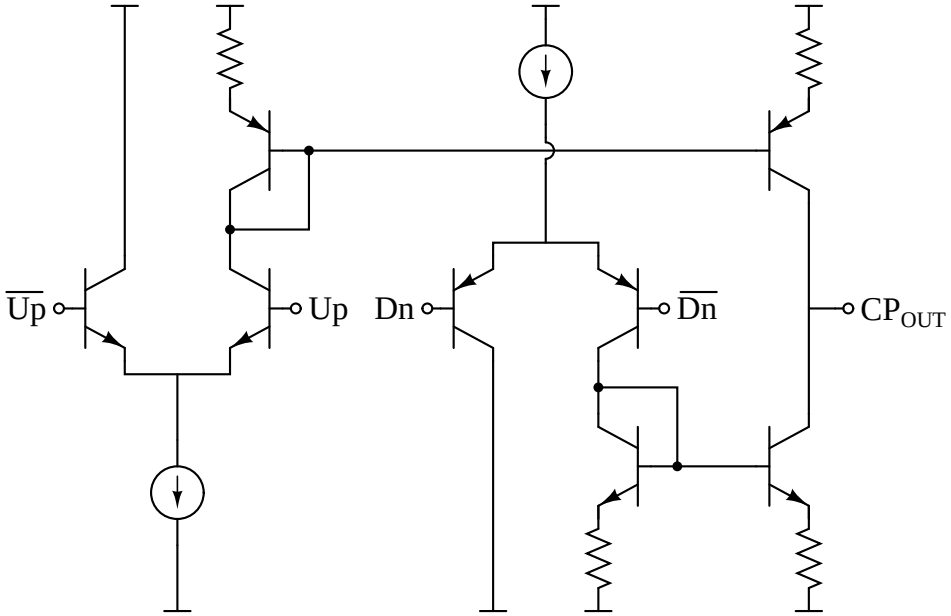


Figure 55: Current-steering charge pump design using SiGe HBTs. Post-radiation leakage is reduced in this design by removing the need for MOSFET devices at the expense of higher pre-radiation leakage.

irradiated to a maximum of 300 krad(Si), which roughly corresponds to a worst case dose accumulated over a 20 year lifetime for a satellite application. The charge pumps were tested under two operating conditions. The first was under a constant tri-state condition, which is similar to charge pump behavior in a locked PLL. The second condition was for a constant sinking of current, which might occur if something were to disturb the loop beyond the pull-in range and the PLL remained unlocked for a significant period of time. Figure 56 shows the tri-state leakage results when irradiated under tri-state, the commonly expected operational condition. Tri-state leakage indicates a degradation in switch isolation from Figure 53. These results show that the output characteristics of the HBT charge pump overlay for pre-radiation and post-radiation conditions at a current leakage of approximately 350 pA. This is higher than the pre-radiation leakage of the standard design, but less than the 1 nA leakage measured post-irradiation, indicating an improvement in post-radiation leakage using the HBT design approach. Surprisingly, the EGL design degrades with

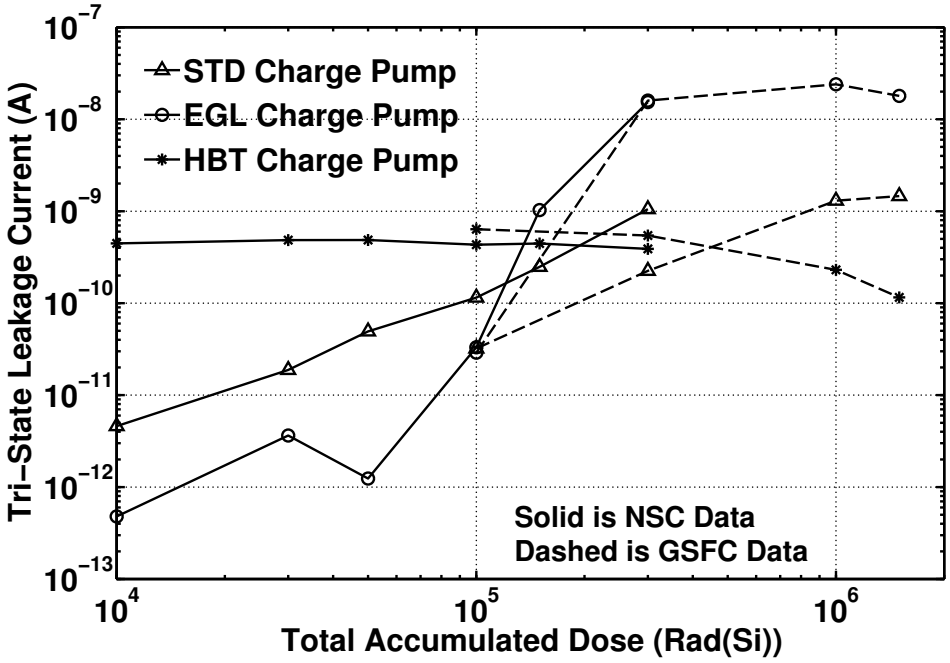


Figure 56: Tri-state current leakage for each design as a function of accumulated dose. Note that the annular layout design (EGL) fails to mitigate and actually exacerbates tri-state leakage.

radiation more than the control design, although tests of the individual devices show no radiation-induced leakage. When exposed in a constant current sink state, the HBT maintains similar characteristics, but the FET based solutions increase their post-radiation leakage by nearly two orders of magnitude, indicating a reduced lifetime when FET-based charge pumps remain in an unlocked condition for long periods of time.

Unlike the degradation in switch isolation, the expected increasing mismatch between sinking and sourcing current did not appear in the measurements. Figure 57 shows simulated and measured current magnitude of the charge pump output characteristics under sinking and sourcing conditions. The simulated results were obtained by integrating worst-case TID device data (strong inversion across the gate) with the BSIM3 model provided by the design kit. In reality, the current sources operate with very modest inversion, which seems more comparable to all-grounded device

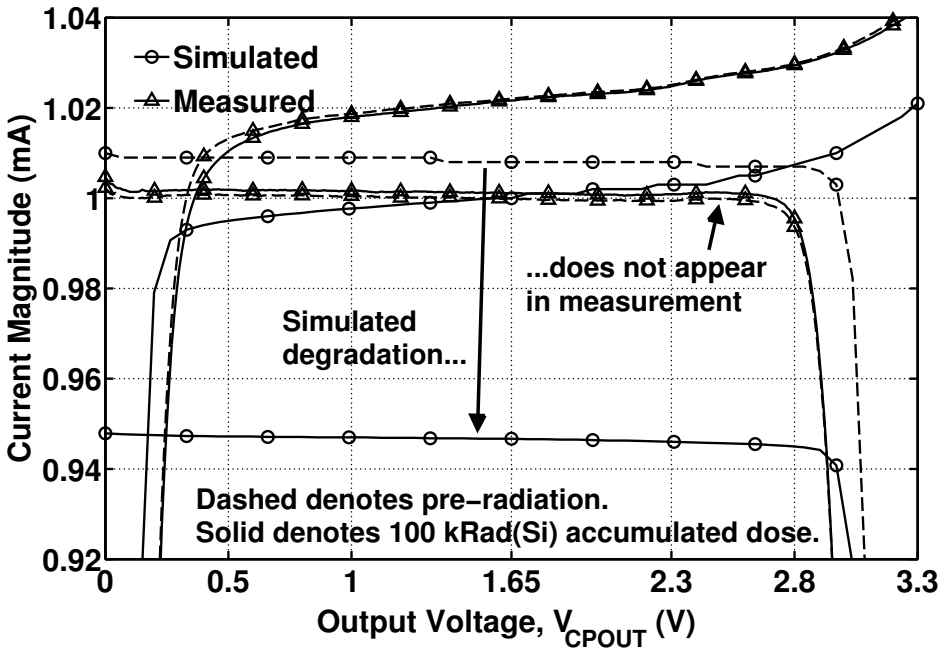


Figure 57: Simulated degradation in current mismatch does not appear in measurement. The cause stems from digital-oriented device characterization being applied to analog models.

measurements.

4.3.3 Single-Event Implications

The design mitigation techniques employed here focus on TID effects, but their impact on single-event effects (SEE) are also important. The CBC-8 platform used in this study employs a thick-film silicon-on-insulator (SOI) process flow, which has been demonstrated to reduce charge collection from a heavy ion strike relative to a comparable bulk process [96]. Traditional single-event cross-section curves are based on the total number of errors encountered. This metric is sufficient for digital circuits where the magnitude of any given error is fixed, but analog circuits require an additional metric to gauge the magnitude of the impact on a continuous system. From the derivation in [62], it becomes apparent that the total excess charge put on to the loop filter will be the appropriate magnitude metric for the charge pump, which will be addressed further in the final paper. Measurements were conducted at the Texas

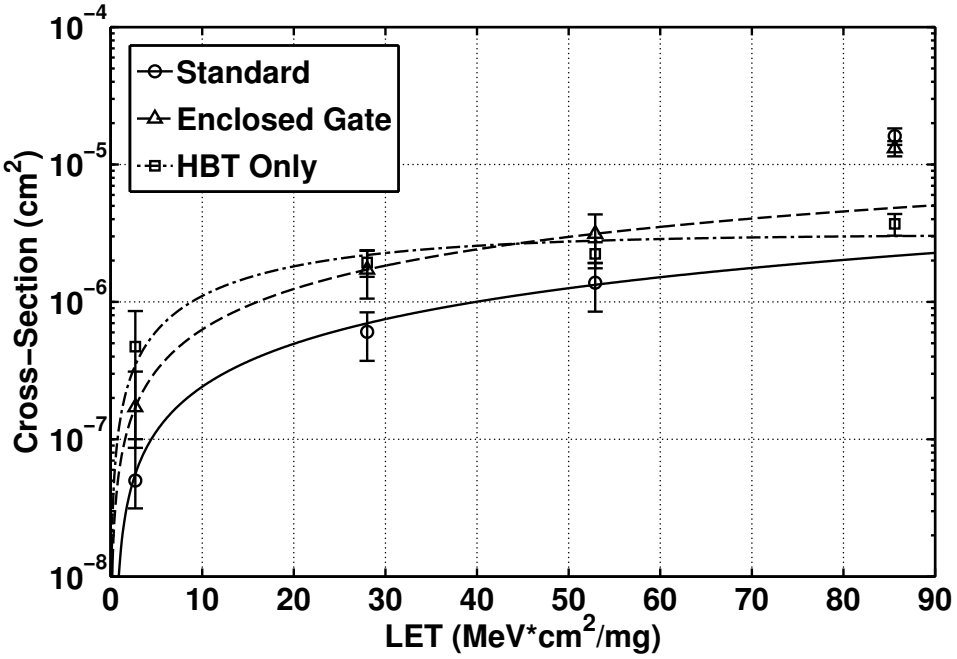


Figure 58: Error cross-section of the three charge pump designs. The HBT design shows a higher susceptibility to errors at low LET, but the use of SOI gives all designs a low cross-section.

A&M cyclotron with cross-section data shown in Figure 58. Despite its significantly smaller die area, the HBT shows a higher cross-section at low LET, although all three designs have a cross-section less than 1x10^6 cm^2 because of the buried oxide layer of the SOI processing. Additionally, the average magnitude of strikes on the HBT design are nearly twice as large as those on the FET-based designs, and also have a much more significant spread of values. The results of this study indicate that complementary SiGe HBTs are effective at mitigating TID degradation of PLL charge pump circuits at the expense of larger transients. Additionally, the use of an SOI process can reduce the frequency of such transients.

4.4 Characterization of Oscillators

As autonomous circuits, oscillators are unique in communications systems. The role of most other primary analog or RF circuits in a communications system are designed for signal conditioning and translation, which means they perform some defined function

on a provided input and output the result. These circuits are typically implemented as linear time-invariant (LTI) blocks to simplify analysis and design. In contrast, oscillators have no input and generate their output signals from internal noise. The desired response as well as requirements to limit the positive feedback make these circuits both non-linear and time-variant. This makes the study of oscillator response to a single-event transient separate from other analog transients such as those considered for charge pumps or other LTI circuits found in the literature [9].

Several studies exist in the literature that have explored single event effects (SEEs) in free-running oscillators as well as complete PLL systems [8,10–12,53,60–62]. These studies cover both ring oscillators and resonant tank oscillators. Ring oscillators are based on digital inverters that are cascaded and fed back in an unstable configuration, producing a periodic waveform based on the delay around the "ring". These circuits are not well-suited for frequency synthesis, since the waveform generated by the oscillator typically includes large spurious harmonic components that would propagate throughout the RF path. On the other hand, resonant tank oscillators produce their output by satisfying the second-order differential equation produced by the series or shunt combination of inductors and capacitors. These circuits are more relevant to frequency synthesis and the studies relating to resonant tank designs can be found in [10–12, 53].

This section summarizes the theory developed to understand the physical processes of the observed transients in resonant tank oscillators, first presented in [36]. The analysis considers effects in the time-domain, providing supporting measurements of an example design, along with an analysis of design implications for transient mitigation. The understanding derived from this theoretical base is important for developing more important relationships between transients and BER in Section 4.5. The theory presented makes no distinction between SiGe or MOS oscillators, but provides the framework for such an analysis in the future. In this case, the oscillator designs

measured to confirm the theory were the same as those presented in Section 3.1.

There are several reasons why a fundamental theory describing SET response for this class of circuits is desirable beyond process technology and circuit-specific observations. The primary motivation is to provide a solid foundation for the development of ideas to mitigate SETs. It can also be used to simplify the prediction of oscillator transients without the need for complicated circuit or mixed-mode simulations.

4.4.1 Developing SET Theory

In order for an SET to impact the output of a resonant tank oscillator, the circuit must be disturbed from its limit cycle. For the cross-coupled negative resistance oscillator considered here, this state information is contained in the voltage across the tank capacitor, making the relevant phase plane variables $v_c(t)$ and $\dot{v}_c(t)$. The simplified model of a negative resistance oscillator developed in Section 1.2.1 is an excellent starting point for understanding transient mechanisms. In the context of integrated circuits, SETs are generated by collisions with energetic ions, which create carriers in the semiconductor material upon impact. The generated track of charge influences circuit operation when it is swept into critical nodes. SET charge flow is therefore modeled as a time-dependent current denoted as $i_{str}(t)$ in Figure 59, with t' used to indicate the instant of charge injection into the tank.

Assume the total charge collected from an SET is injected instantaneously into an oscillating resonant tank in steady-state, such that it can be modeled as an ideal charge step. This step corresponds to a Dirac delta function in current, which is the time-derivative of charge. The inductance in the resonant tank will resist this sudden change in current, so all of the charge will be placed across the capacitor. Here, the charge is translated to voltage through the definition of capacitance such that

$$\Delta v_{str} = \frac{\Delta q}{C}. \tag{81}$$

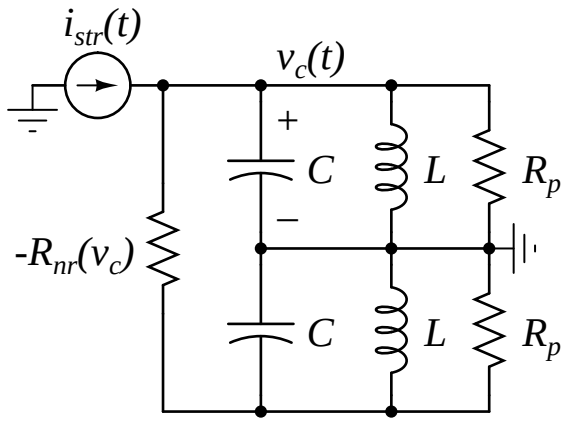


Figure 59: The simplified model of a negative resistance oscillator developed in Section 1.2.1. A time-dependent current source, $i_{str}(t)$, representing the carrier flow generated by an ion strike is added.

This voltage step will add via superposition with the steady-state voltage across the capacitor at time $t = t'$. Since the steady-state voltage is periodic in time, the transient characteristic observed will be dependent on the relative phase of the signal at the moment of the strike. Meanwhile, the $\dot{v}_c(t)$ condition will remain unchanged as the derivative of the voltage step will again become a Dirac delta function, zero for all time except the instant $t = t'$. Thus, the state change from the injection of an ideal charge step can be written as

$$v_c(t'^+) = v_c(t'^-) + \Delta v_{str} \tag{82}$$

$$\dot{v}_c(t'^+) = \dot{v}_c(t'^-). \tag{83}$$

The visualization of this response in the phase plane can be seen in Figure 60. The state of the oscillator can be represented by a 2-dimensional vector, $\vec{S}$, combining the $v_c(t)$ and $\dot{v}_c(t)$ conditions. In steady-state, $\vec{S}$ will be periodic and as such can be determined as a function of its angular position, $\omega_0 t$. The ion strike that produces Δv_{str} produces two distinct effects on $\vec{S}$. The first produces a change in phase and hence angular position denoted by $\Delta\phi$ in Figure 60. Under the assumption of an ideal charge step, this phase change will be instantaneous. The second effect is a

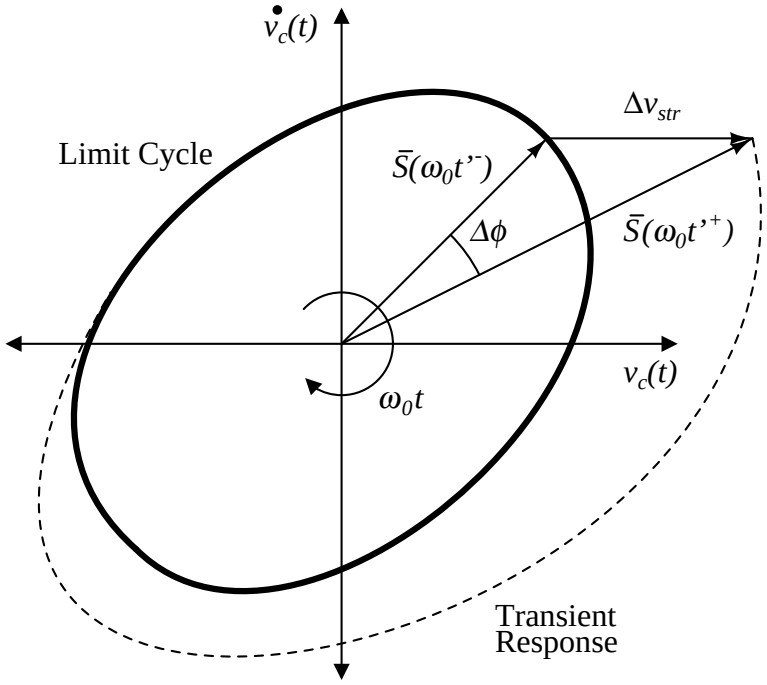


Figure 60: A phase plane visualization of an ion strike that can be approximated by an ideal charge step. The variable t'^- represents the time infinitesimally prior to the step, while t'^+ represents the time infinitesimally after the step.

change in the magnitude of $\vec{S}$ that requires a return to the limit cycle dependent on the dynamics of the system. The dashed line in Figure 60 is representative of the path the system takes through phase space as it returns to the limit cycle.

Simulations of the ideal charge step were done using a narrow current pulse that injects the appropriate amount of charge into the tank. The single-ended results of this simulation can be seen in Figure 61. Careful distinction between single-ended and differential results are needed because the anti-phase condition is not necessarily upheld during a transient on one side of the circuit. This relative phase shift can reduce the effective voltage when observed differentially. If observed in a single-ended fashion, the output of the cross-coupled oscillator will be equivalent to $v_c(t)$, and will simply be a projection of $\vec{S}$ onto the x-axis. The simulations show two different observable characteristics: a "bulge" characteristic for transients that move the state of the system outside the limit cycle, and a "dip" characteristic for transient states

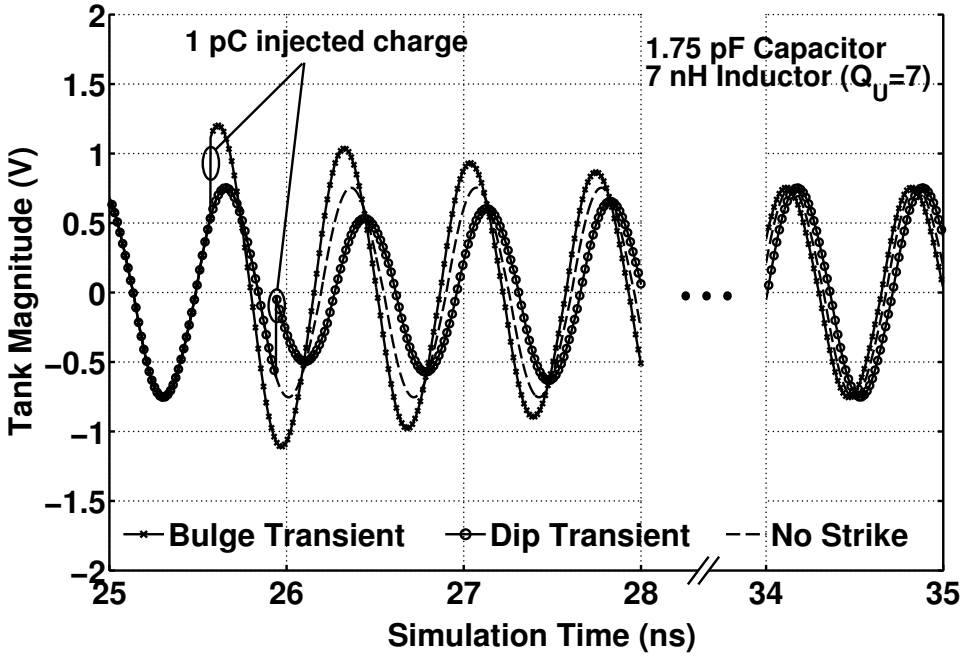


Figure 61: Simulations of transient response to an ideal charge step. The two transients shown represent injections of equal charge and highlight that the observed response will depend on the relative phase of the oscillating waveform at the time of the strike.

inside the limit cycle. Note that as the system returns to steady-state, the phase shift introduced by the SET at $t = t'$ remains. The type and degree of the characteristic observed will depend on the magnitude of the injected charge as well as the relative phase at the time of the strike.

To this point, the treatment of SETs has been similar to the general argument formulated by [32] to explain noise phenomena in oscillators. The concept of the linear time-variant (LTV) impulse response employed by that analysis is also used here to gauge the magnitude of SET response. The phase impulse response has been defined as

$$h_\phi(t, t') = \frac{\angle\vec{S}(\omega_0 t'^-) - \angle\vec{S}(\omega_0 t'^+)}{\|\vec{S}\|_2} u(t - t') \tag{84}$$

in [32] where $u(t)$ is the unit step function, while the amplitude impulse response has

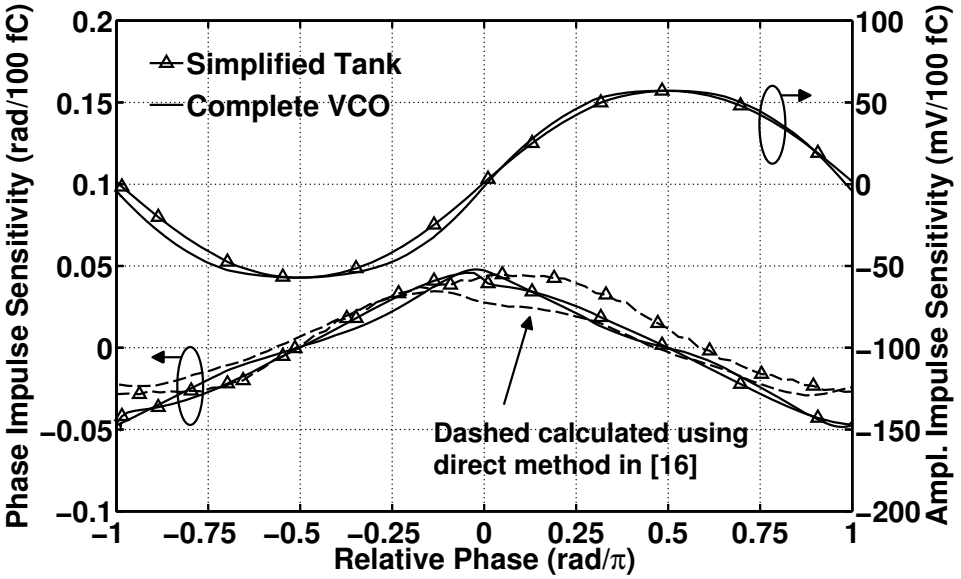


Figure 62: Phase and amplitude sensitivity of the circuits in Figure 59 and Figure 23 to a current impulse. The injected current is equivalent to a strike on one of the cross-coupled devices directly connected to the resonant tank. The functions are time-variant and periodic equivalent to the period of oscillation.

been defined as

$$h_A(t,t') = \frac{|\vec{S}(\omega_0 t'^{+})| - |\vec{S}(\omega_0 t'^{-})|}{\|\vec{S}\|_2} e^{-\frac{\omega_0 (t-t')}{Q}} u(t-t') \tag{85}$$

in [56], where the exponential term captures the decay of the amplitude disturbance for oscillators with low to moderate Q resonators typical of IC designs. The effects of amplitude fluctuations are often neglected in noise analysis because they are suppressed by the internal self-limiting nonlinearity. However, the external stimulus provided by an SET makes amplitude modulation a significant consideration, as demonstrated by [11]. In order to calculate both the magnitude and phase change of $\vec{S}$ due to a charge step, a phase plane estimation method is used that takes the normalized steady-state phase plane response and applies the conditions outlined in (82) and (83) to estimate a strike. These results are shown in Figure 62 overlaid with the direct calculation method outlined in [32]. The results are reasonably close.

For SETs that can be modeled as an ideal charge step, the sensitivity functions

shown in Figure 62 represent the excess amplitude and phase one could expect to observe from a physical transient. This assumption will hold for pulse durations that are significantly less than the period of oscillation. However, when the transient duration and oscillation period are of the same order, a superposition integral that shifts relative to the strike time, t', and given as

$$\Delta\phi(t,t') = \int_{-\infty}^{\infty} i_{str}(\tau) h_{\phi}(t, \tau + t') d\tau \tag{86}$$

must be used to determine the shape of amplitude and frequency transient fluctuations over time. Here, $i_{str}(t)$ is used to represent the injected current over time. Note that a Dirac delta function for $i_{str}(t)$ causes the transient response to be a scaled version of the impulse response. A similar calculation is used for $\Delta A(t,t')$. Calculating this integral can become tricky as the time-variant sensitivity functions must maintain linearity in order to fully characterize an arbitrary input function. Figure 63 shows the linearity characteristics for the amplitude and phase sensitivity. Note that measurements of device transients in Figure 64 indicate a total injected charge, q_{tot}, over twice as large as the values shown in Figure 63. However, it is not the total injected charge but the individual charge steps that are important. From the current waveforms shown, the peak charge injected per time step of the oscilloscope for the largest transient is approximately 160 fC, still within a reasonably linear range of Figure 63.

4.4.2 Defining Oscillator Figures of Merit

The preceding theory has developed a method to calculate the time-dependent amplitude and phase deviations from an SET that fit a solution to the primary harmonic of (22) in the form

$$v_c(t,t') = (A + \Delta A(t,t')) \cos(\omega_0 t + \Delta\phi(t,t')). \tag{87}$$

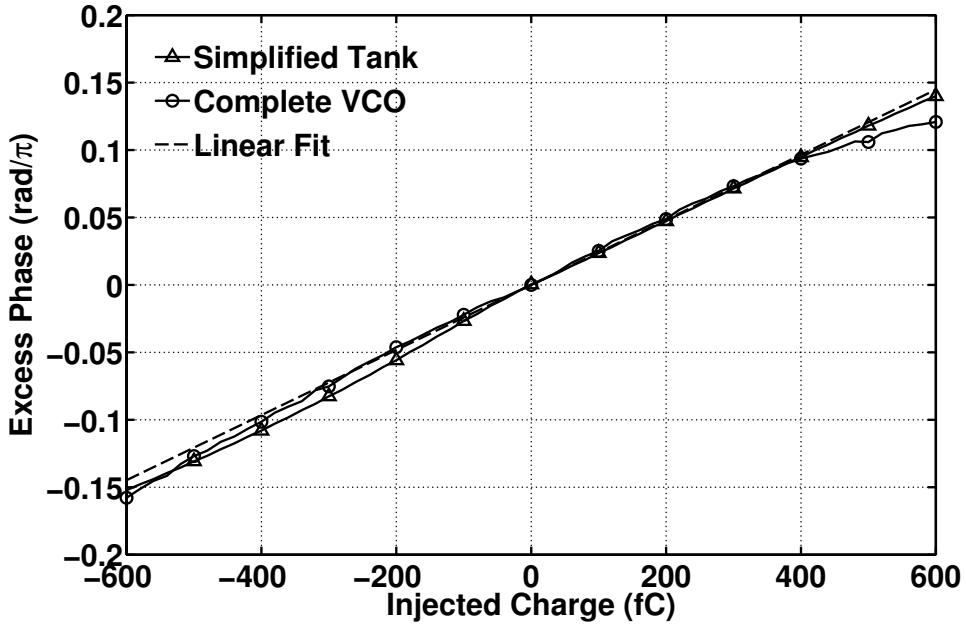


Figure 63: Linearity at zero crossings of the output voltage waveform, which will be the worst case condition for linearity. This condition is only required when the SET cannot be modeled as an ideal charge step.

This information is only one piece of the puzzle when considering the implications of SETs on system performance. The time, location, and magnitude of an ion strike will all be random variables in an operating environment. Traditional metrics such as the error cross-section curve provide statistical information on these variables by normalizing the time and location variables into an "effective" sensitive cross-section with units of area. Similar to other analog circuits such as the charge pump, a metric for the magnitude of a transient response is also desired. However, the time-dependent nature of the oscillator's impulse response adds a level of complexity not yet considered.

Using the transient response functions, $\Delta\phi(t, t')$ and $\Delta A(t, t')$, several observable figures of merit (FoM) describing the transient can be established. First, consider the metric of total phase displacement used in [61]. For a resonant tank oscillator this can be defined as

$$\Phi_e\big|_{t'=t_n} = \lim_{t\to\infty} \Delta\phi(t, t_n). \tag{88}$$

The other FoM that will be considered here is transient duration. This can be defined as the time it takes for the change in both $\Delta\phi$ and ΔA to settle to within some threshold, ϵ, around zero. This is expressed mathematically as

$$D_e\big|_{t'=t_n} = \max(t_{\phi,max} - t_{\phi,min}, t_{A,max} - t_{A,min}) \tag{89}$$

where

$$t_x \in \left|\frac{d}{dt}\Delta X(t, t_n)\right| > \epsilon. \tag{90}$$

The strike instant for a given sample, $t' = t_n$, is independent of the relative phase of the oscillating signal, and therefore the probability of a strike occurring at a given phase will have a uniform density across the normalized period of oscillation, $(-\pi, \pi)$. The deterministic FoMs defined in (88) and (89) can be combined with the probability density for the VCO phase at strike time to form a probability density for the FoM. This can be determined by plotting the histogram of the FoM where each time point is considered a "sample". These distributions will not have a traditional characteristic, such as Gaussian or Poisson, and therefore box plots are used when plotting predictions for these FoMs across energy levels such as linear energy transfer (LET).

4.4.3 Confirmation of Theory via Measurement

The oscillator designs used to test this theory were the same as those used to analyze phase noise of the IHP complementary process in Section 3.1. Similar transient characteristics were observed in both the *pnp* and *npn* designs, therefore data is presented only on the *pnp* VCO for brevity. Transients were injected into the oscillators through carrier generation by two-photon absorption using a Ti:Sapphire regenerative

amplifier at the Naval Research Laboratory. A backside technique was used to allow precise Z-axis control of the generated carriers as well as prevent undesired reflection and optical scattering from routing layers on the top side of the design [66]. The oscillators were packaged with the die mounted and bonded directly on a custom-built PCB using a Rogers 4003 dielectric to reduce attenuation of the high-speed transients. The relevant transistors were aligned over a via to allow laser penetration through the back side of the die. To provide the clearance necessary to focus the laser on the back of the die, the alignment via was beveled from the back side by hand using a drill bit. This method represented a significant increase in circuit integration capability as well as cost reduction over previous methods that involved machining precision metal fixtures for individual devices [73].

Single event effects were observed in the time-domain in a free-running condition. A Tektronix DPO71254 real-time 50 GS/s oscilloscope was used to capture data by passing each end of the VCO's differential output signal into a separate channel. The oscilloscope was triggered using an external TTL line tied to the pulse repetition rate of the laser.

A manual scan around the die reveals several sensitive areas within the cross-coupled VCO circuit, with emitter-center strikes on either of the cross-coupled SiGe HBTs producing the strongest transients in all design variants. Strikes on passive devices such as the resistors, inductors, and MIM capacitors produced no transients. Surprisingly and for reasons still unknown, strikes on the pn-junction varactors also produced no transients using the two photon laser. Laser energy was varied from 1 nJ to 10 nJ, which was determined to approximately correlate to space-relevant particles with a maximum LET of 100 MeV-cm^2/mg based on direct comparisons using SRAM cells [65]. The laser energy holds a roughly quadratic relation to LET.

The nodes of the transistor that will inject charge into the resonant tank for this circuit topology are the collector and base. The SET response on the collector of

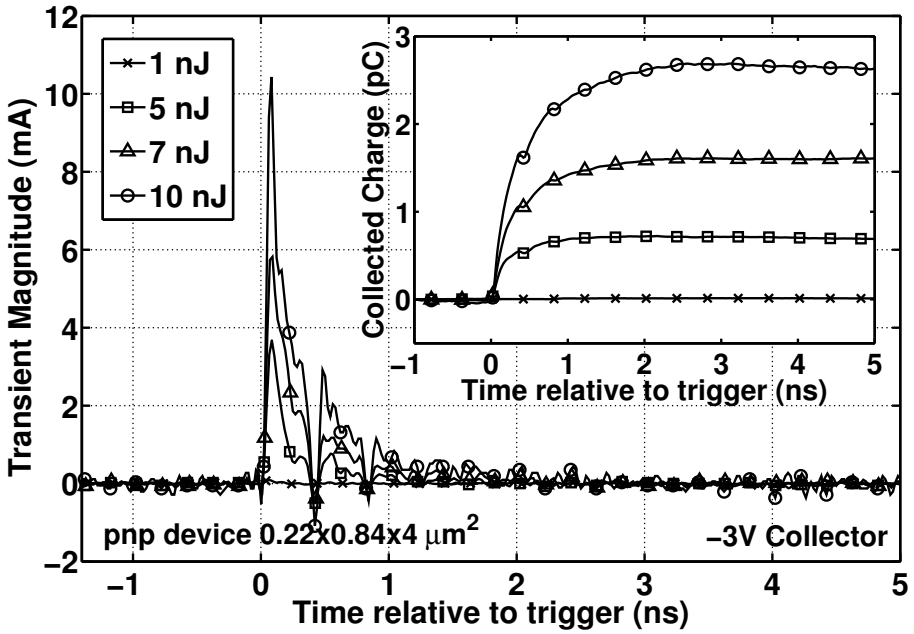


Figure 64: SET response of the collector node of a single *pnp* SiGe HBT. The inset is the integrated current waveform revealing a function similar to a step function.

an individual *pnp* HBT can be seen in Figure 64. This node will dominate since the base response is several orders of magnitude smaller than the collector. The current was determined by reading the voltage across a 50Ω resistor. Integrating the current across time reveals the accumulated charge from the strike. Note that when accumulated, the injected charge resembles a step function with a rounded edge. However, the duration of the pulse at approximately 1 ns is on the same order as the oscillation period at 1.4 GHz. Equation (86) must therefore be used to calculate the transient response functions. The device transient waveforms in Figure 64 do not have significant diffusion tails, so a simple double exponential function,

$$i_{str}(t) = \frac{q_{tot}}{\sigma^2} t e^{-t/\sigma}, \tag{91}$$

reasonably estimates the shape of the current where q_{tot} is the total charge injected and σ is a parameter fitted to the data defined as the rise time from the strike instant, t', to the peak of the waveform.

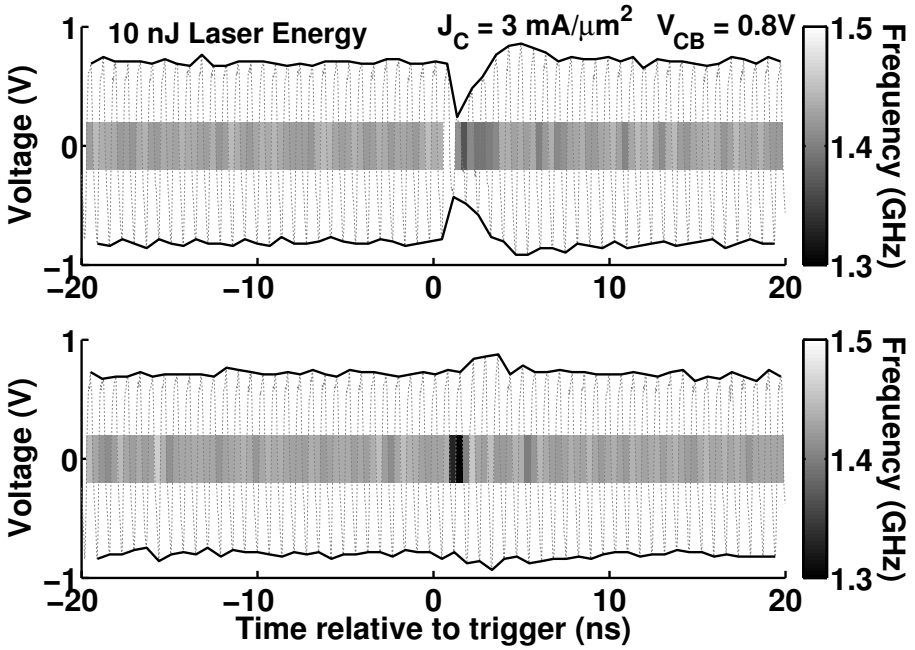


Figure 65: Measured SETs highlighting both "bulge" and "dip" amplitude characteristics. The intensity bar represents an estimate of the frequency averaged over one period as determined by zero-crossings in the data. Note that the brief frequency delta marks a step in the phase of the signal.

Emitter strikes on one of the cross-coupled SiGe HBTs are considered first. An example of two typical transient waveforms observed at identical locations and energy levels can be seen in Figure 65. The dotted line is the raw measurement from the oscilloscope, while the solid line helps to visualize the amplitude envelope of the VCO output. Similar to the observations made in [53], the transients can be empirically sorted into "bulge" and "dip" categories based on the shape of their envelope. However, equally important to this analysis is an estimation of the frequency during the relevant transient cycle. The intensity bar across the waveforms in Fig. 65 represents the frequency averaged over one period. This is accomplished by detecting both the rising and falling zero crossings of the transient waveform and taking the inverse of the time difference between rising pairs and falling pairs. The result shows a delta-like response in frequency near the time of the strike corresponding to a step-like response in phase. This supports the theory that an SET will produce both amplitude and

phase modulation in the oscillator and shows the same time-variant characteristics as the predicted simulation results in Fig. 61.

To calculate the FoM estimations derived previously at the peak laser energy of 10 nJ, first apply the current waveform estimated by (91) using $q_{tot} = 2.6$ pC and $\sigma = 82$ ps from Figure 64 to the sensitivity functions (84) and (85) using (86). This gives the transient response across time, t, for all possible strike times, t'. In this case, (86) was evaluated numerically in MATLAB and stored as a two-dimensional array. FoMs such as those defined in (88) and (89) are then used to collapse the transient responses into a single number at each possible strike instant across the period, effectively reducing the two-dimensional matrix to a one-dimensional function of t'. Using the random nature of the SET, a probability distribution for the magnitude of the FoM can be derived using its histogram normalized to the number of time points in the simulation. The resolution of the probability density is directly dependent on the number of time points, or samples, used to calculate the sensitivity functions. This process is then repeated for the other energy levels.

This calculation for the total phase displacement metric can be seen in Figure 66. Transient duration data can be found in Figure 67. Measured data points have been overlaid for reference. Note that the statistical transient duration estimates contain several outliers that produce short duration transients at nearly every energy level. Since there were 80 total samples to determine the probability distribution, this would indicate that roughly 5% of transients will produce a significantly shorter disruption simply by striking at a fortunate instant during the oscillation cycle.

In measurement, a third classification of transients were observed that caused a sustained collapse of the oscillation for several periods. These transients occurred intermittently only at large laser energies and have been observed in other works, but are not modeled by the developed theory [10, 53]. Recall that sustained oscillation requires the negative resistance provided by the cross-coupled pair. The designed

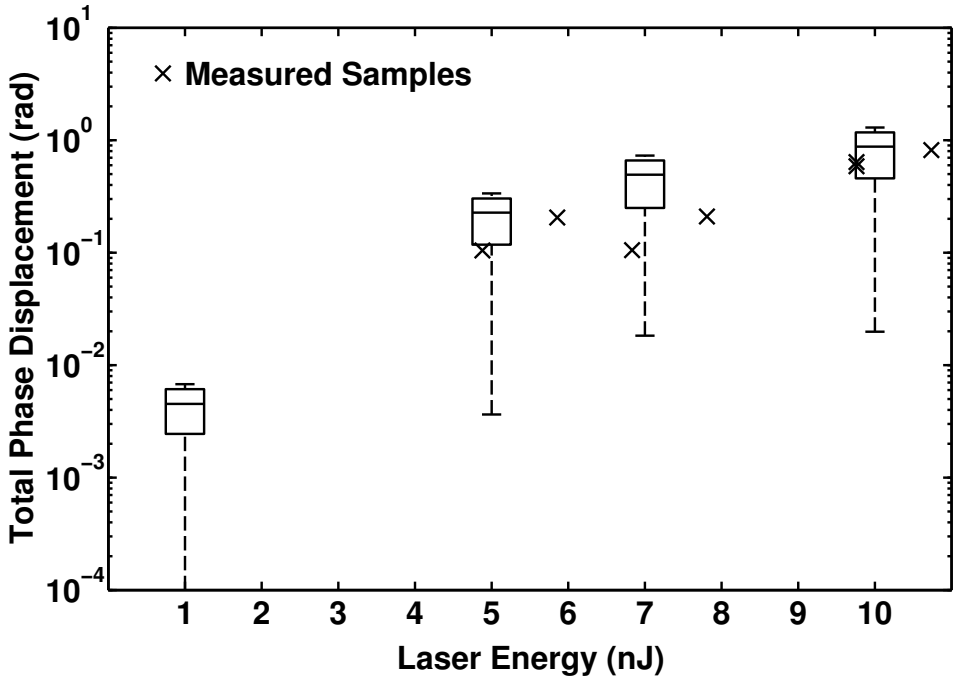


Figure 66: Total phase displacement across laser energy. The range of predicted values are given as box plots, where the box denotes median, first quartile, and third quartile. The whiskers denote data extents. Individual marks note measured samples.

negative resistance operates on the assumption that the transistors operate in the forward active mode. The vector diagram in Figure 60 shows that a strike near the maximum of $v_c(t)$ will produce an even larger voltage across the capacitor, which also determines V_{CE} across the cross-coupled transistors, resulting in a "bulge" style transient. If enough charge is injected during this strike, the voltage will go beyond the breakdown threshold $BV_{CE}(Z_S)$, where Z_S is the time-dependent input impedance of the device. Beyond this point the transistor will move into the breakdown region of operation and can no longer be characterized by (21). Once the transistor crosses this threshold, measurement evidence suggests that the collapse observed will always be the same duration. Because these transients are significantly longer than the smaller modeled transients, they should be avoided through design as discussed in Section 4.4.4.

A final consideration of interest involves strikes on the tail-biasing transistor,

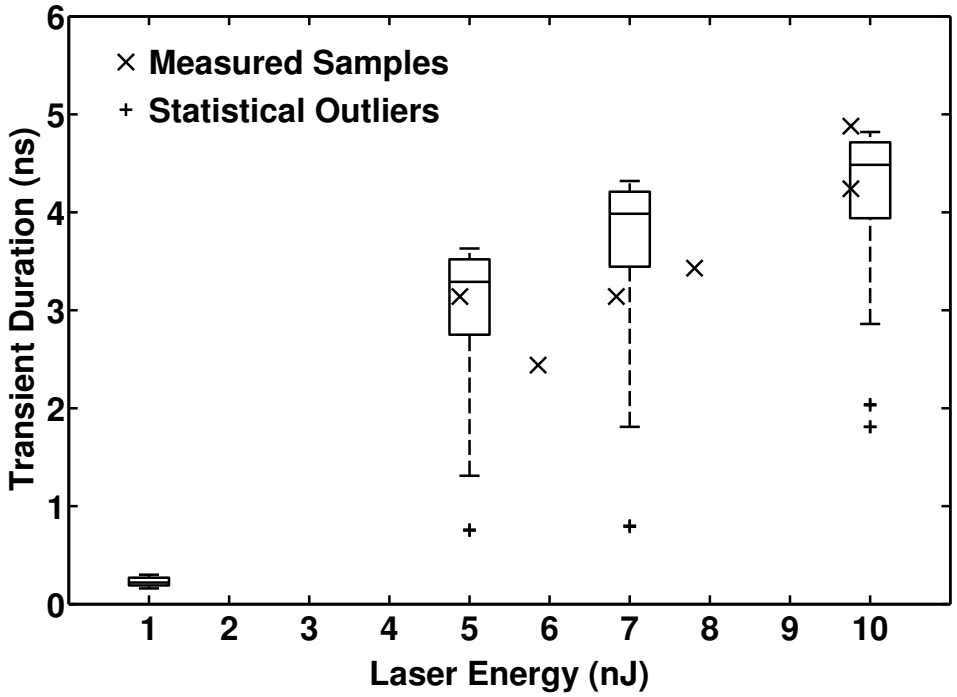


Figure 67: Transient duration across laser energy. The range of predicted values are given as box plots, while marks denote measured samples.

Q_3. Measurement observations reveal that strikes on this node produce generally smaller transients than those on the cross-coupled transistors, Q_1 and Q_2. Simulations for total phase displacement using ideal charge step injections on the full oscillator schematic reveals in Fig. 68 that the phase sensitivity has half the period of injections on the cross-coupled transistor, clearly implicating common-mode rejection (CMR) as the mitigating factor. This can be confusing, as a Dirac delta that occurs while one of the transistors is off should intuitively be translated directly to the tank node, producing similar transient levels. However, even though the charge injection is very brief, the full circuit schematic contains a number of parasitic resistances that introduce RC time constants that smear the charge across time. At the oscillation frequency of 1.4 GHz, the time constants involved are such that strikes anywhere in phase are spread in time enough to encounter CMR during at least one of the two switching instants that define the oscillation period. The observed effect is therefore

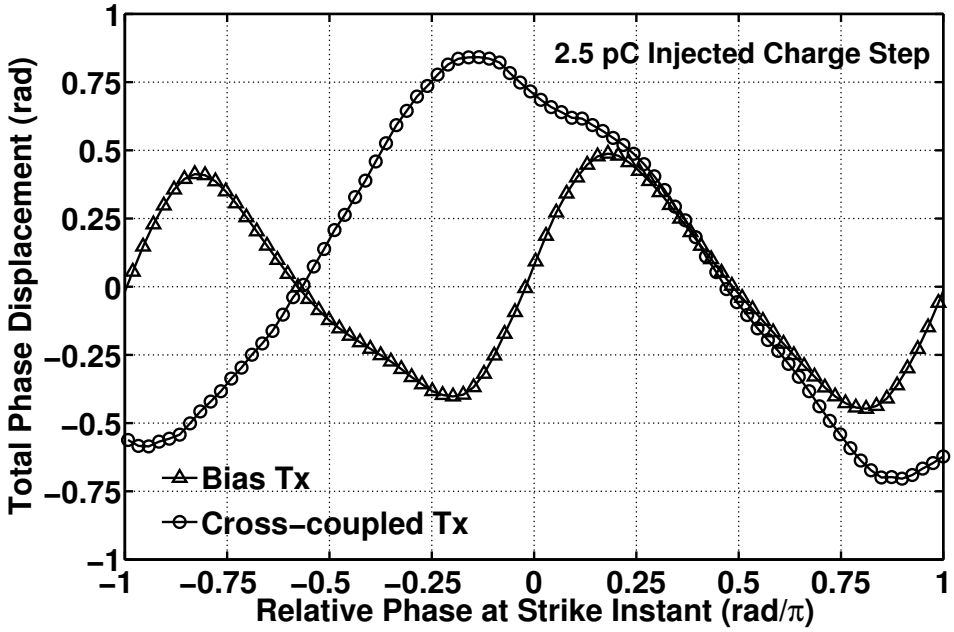


Figure 68: Total phase displacement simulations across strike instant revealing strikes on the biasing transistor, Q_3, produce smaller transients via common-mode rejection. This is confirmed by measurement observations.

both technology and frequency dependent, and not a general statement of transient effects in all cross-coupled oscillators. Oscillations at a lower frequency, or a technology or layout with lower parasitic capacitance, may not stretch the injected charge long enough to encounter CMR.

4.4.4 Design Implications

Understanding the physical implications of SET phenomena on resonant tanks provides several key insights into potential mitigation techniques that might otherwise go unnoticed. First, it is advantageous to maximize the charge displaced by the tank capacitance. Resonant frequency is an under-determined system made up of an inductance, L, and capacitance, C, so there are multiple solutions that provide the same frequency. Because the magnitude of the voltage step is determined by the relation in (81) it is thus advisable to choose the largest capacitance possible to make up the tank so that transient impact is minimized. Figure 69 demonstrates this

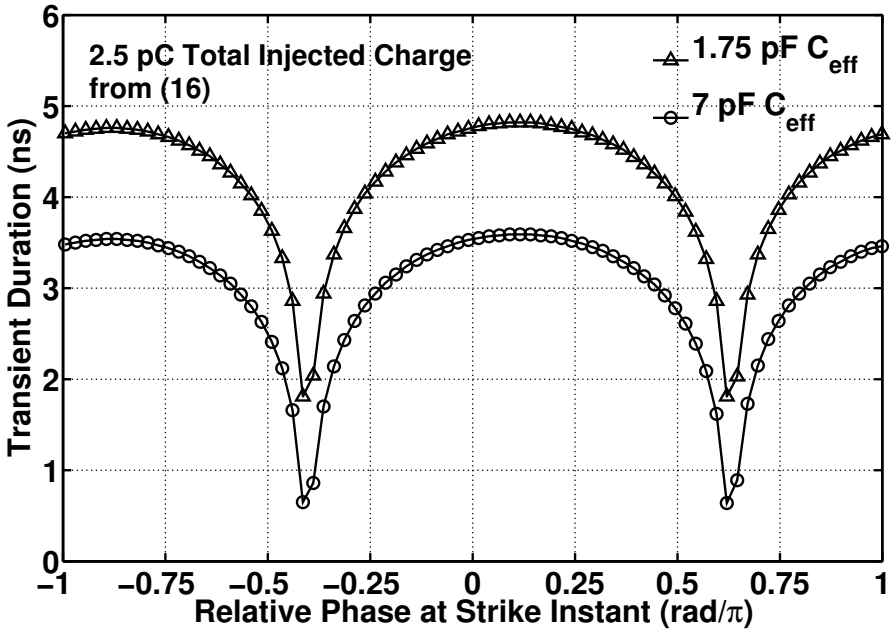


Figure 69: Transient duration decreases for a comparable injected charge as the effective tank capacitance increases.

effect by increasing the effective capacitance on the tank node by a factor of four and observing a corresponding decrease in transient duration of approximately 1.5 ns. By reducing Δv_{str}, this technique can be most useful in ensuring that the oscillator does not exceed the breakdown threshold that produces long collapse transients.

The theory also suggests a trade-off in the desirable quality factor, Q, of the resonant tank for applications that require single-event considerations. Typically, higher Q is desired in order to minimize phase noise [32]. While this still remains true, (85) reveals that higher Q will also increase transient recovery time by scaling the exponential function. Therefore, resonator Q is a good tuning knob for reducing transient duration at the expense of phase noise.

Several indicators of frequency scaling have also been identified. For low frequency oscillators with periods much larger than potential SET pulse widths, SET modeling can be simplified to a Dirac delta-like brevity. By not stretching out over a larger region of the periodic sensitivity functions, this suggests lower frequency oscillators

will encounter much larger variability to SETs based on the strike time relative to periodic phase. Also, as resonant frequency increases, the LC combination that makes up the resonant tank will decrease. The limited range of practical L and C values will inevitably put downward pressure on total tank capacitance, meaning a greater voltage change for a given charge. Thus, transient magnitude is expected to increase with the frequency of oscillation.

It is worthwhile to mention that transconductance plays no first-order role in determining SET characteristics. This would seem to indicate no difference between the FET and HBT apart from the shape of $i_{str}(t)$ if necessary. This even footing in circuit response should provide an SET advantage for FET-based oscillators because they are horizontal devices and provide no gain for carriers injected into the channel through the body of the device. Charge tracks in the vertical bipolar device, on the other hand, amplify any generated charge swept through the base. However, the gains in single-event response are more than offset by the significant total ionizing dose problems in MOSFETs, to which HBTs are immune.

4.5 System Level Metrics

The preceding sections have analyzed the impact of single-event effects for many of the circuit blocks comprising the modern frequency synthesizer. However, understanding the impact on circuit blocks alone is not sufficient for a complete strategy for radiation hardness. Radiation tolerance considerations are typically handled first at the system level, with an engineer who understands the mission specifications making decisions about how many bit errors are acceptable over a given period of time. Such metrics are typically determined for a given environment defined in [2]. From this determination, a number of bit errors attributable to the non-idealities of the LO frequency synthesizer must be defined for the signal-to-noise ratio of the received wireless signal. The bit error specification must be translated into acceptable metrics

such as phase noise for circuit design [14]. Only then can mitigation strategies for circuit-level transients be considered.

In the current literature, very little of this understanding exists for radiation hardness beyond early attempts to characterize individual circuits. Particularly troubling is the lack of explanation for the translation of observed SET disturbances to digital bit errors. The efforts outlined here have focused on bridging this knowledge gap. In traditional frequency synthesizer design that does not consider radiation effects, [14] shows that BER can be predicted based on the RMS phase error of the synthesizer output. This single number metric is determined by integrating the SSB phase noise over all frequency. Therefore, our initial efforts to translate ion-induced phenomena focused on the application of frequency domain techniques to the problem. This approach was bolstered by measured results shown in Figure 70, where repetitive laser strikes at a single location and energy produced a consistent response in spectrum analyzer sweeps. A maximum hold function then allowed the envelope of the laser strikes to be determined as a function of location and energy. This envelope could then be used to estimate the RMS phase error, which in turn predicted BER [36].

Despite its relative simplicity, this approach was abandoned for several reasons. Frequency domain results depend on the assumption of steady-state conditions thanks to the bounds of integration in the Fourier transform. In order to reproduce the measured results, this requirement was circumvented by truncating the transient waveform and assuming the waveform was periodic. The Fourier transform of this waveform should approximate the frequency domain response as the period of the repeated waveform increases to infinity. However, the computational expense of this technique grows significantly as this occurs, particularly for close-in offset frequencies, which makes an accurate estimate for RMS phase noise difficult to ascertain.

An alternative method developed here seeks to use time-domain metrics to directly interpret BER from frequency synthesizer transients. Key to this analysis is a

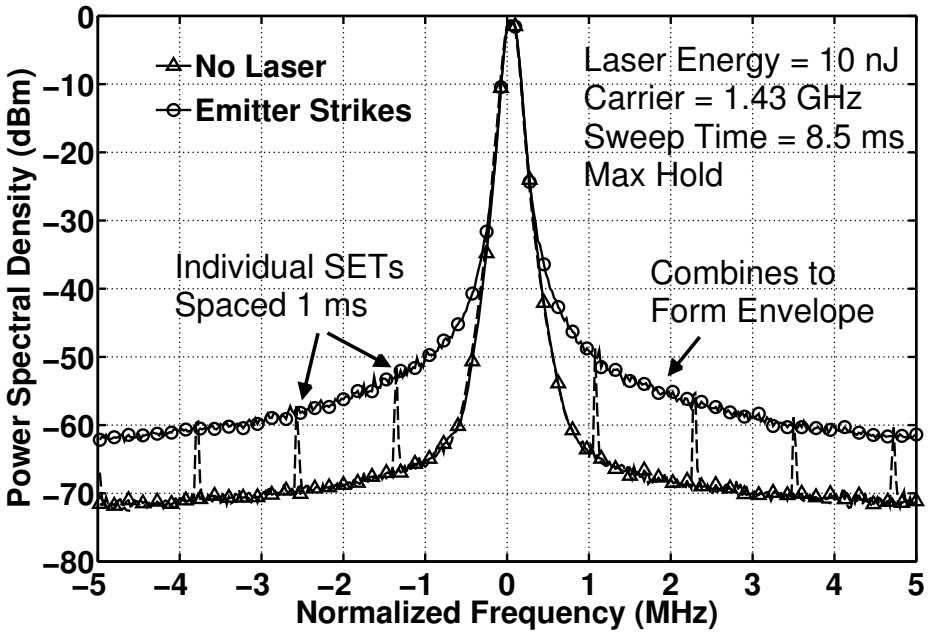


Figure 70: Frequency-domain measurements of SET response in a free-running VCO. Individual laser strikes are held at each point of the spectrum analyzer sweep to form an envelope used to make a coarse estimate of RMS phase error.

recently published paper that presents linearized predictions of transient waveforms for a closed-loop PLL, which is applicable for frequency synthesizers [62]. These equations allow the prediction of transient waveforms at the PLL output for a defined amount of charge injected into a given circuit block based on previous circuit block characterizations. The next step in this process is to translate these predicted waveforms into accurate predictions of bit errors.

We have proposed a direct method for determining bit errors through time domain measurements as shown in Figure 71. This measurement will rely on a broad-beam environment to collect accurate statistics, but since such time is expensive, we have first demonstrated the system using a laser system to emulate the charge tracks generated by a ion. This system is similar to the technique used in Section 4.4, but rather than a two-photon technique, the laser used a single photon greater than the band-gap energy of silicon to produce true charge tracks that are easier to correlate to LET. The drawback here is that metalization layers above the silicon can block the

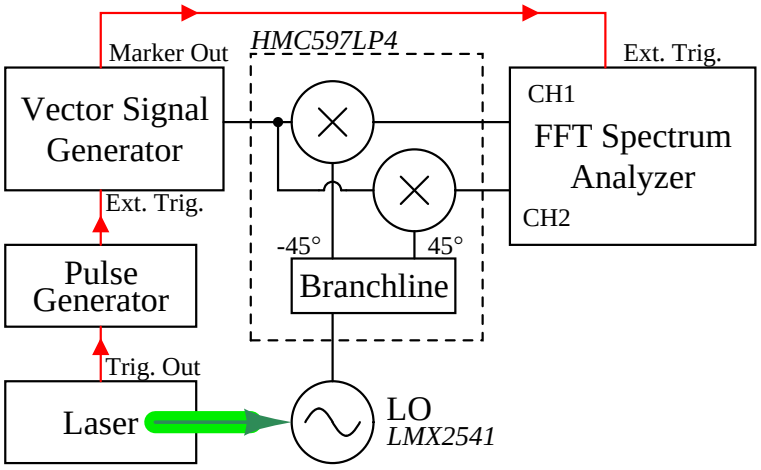


Figure 71: Time-domain measurement setup for BER of a system whose LO experiences an SET.

photons, preventing them from producing charge tracks at all in certain locations.

In the setup used to demonstrate this new concept, a complete transceiver was constructed for direct measurements of BER. The Rohde & Schwarz SMU200A vector signal generator in Figure 71 creates a pseudo-random bit stream and modulates it onto the RF carrier using the desired scheme. A custom-built circuit board contains Hittite down-conversion mixers for coherent demodulation at baseband using in-phase and quadrature channels. The LO for this down-conversion process is the device under test, and for the purposes of the demonstration a National Semiconductor LMX2541 frequency synthesizer is used. This commercial part uses a proprietary 0.25 µm SiGe technology. Since the part is already packaged, the lids of the packaging were etched off to provide access for the photons to the die. The down-converted signal is passed in two channels to an HP89410A FFT Spectrum Analyzer, the same unit used for phase noise measurements in a different mode of operation. In vector measurement mode, the HP89410A acquires the in-phase and quadrature time domain signals in a 10 MHz bandwidth and demodulates the captured signal into digital bits. Thus, with the known pseudo-random bit stream generated and a corresponding bit stream demodulated after passing through the DUT, a simple synchronization routine can

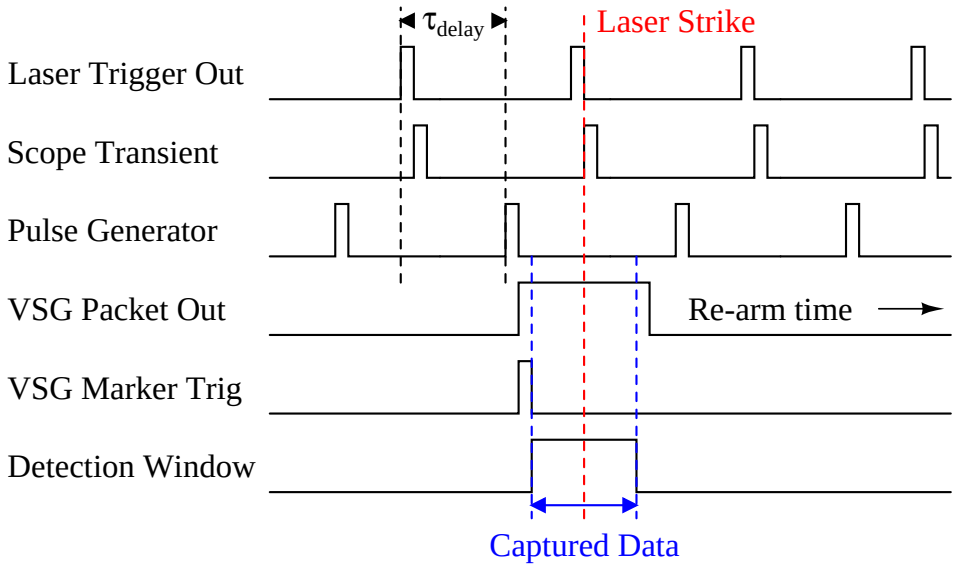


Figure 72: Timing of the BER measurement so that the laser strike occurs in the middle of the transmitted packet.

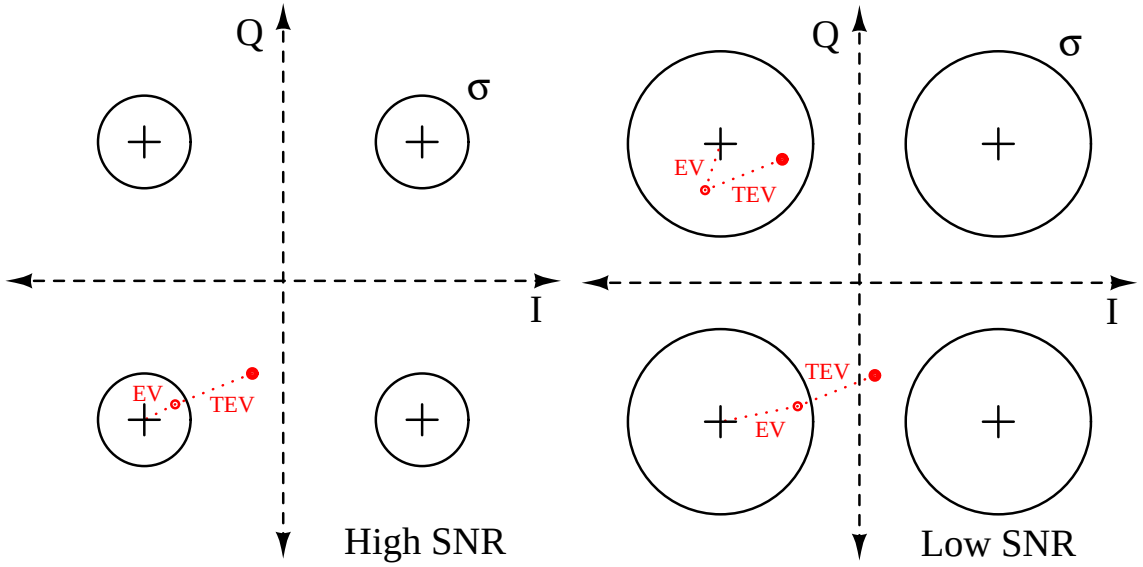
produce the number of bit errors and the BER.

In order to make the desired measurements, the time of the laser strike must be closely coordinated with the transmitted stream of symbols. The laser system outputs a TTL trigger pulse tied to the repetition rate of the laser pulses. As shown in Figure 71, this trigger line is used to trigger the vector signal generator (VSG) to begin transmission of a packet. The FFT spectrum analyzer is triggered and synchronized by the marker output of the VSG. Thus, the triggers are cascaded rather than run in parallel to ensure proper detection of the packet. However, the delay between each of the triggers would mean that the laser would strike the die several nanoseconds before packet transmission begins without an appropriate delay added to the trigger. This delay is provided by an HP pulse generator shown in Figure 71. Thus, the delay was adjusted such that the captured transient was initiated by the trigger pulse from the previous laser strike and positioned approximately in the middle of transmitted packet. The timing of this procedure is shown in Figure 72.

The measurement procedure based on this setup is predicated on observing an

increase in bit errors in the presence of a laser strike. The BER for a system dependent on its signal-to-noise ratio is well known for a variety of digital modulation schemes [85]. In communications systems, signal-to noise ratio is typically represented by the energy-per-bit to noise ratio (E_b/N_0), which in this case can be directly set by the VSG. Therefore, measurements are first taken at a given SNR with no laser present to give a baseline BER measurement. This value should match closely with theoretical predictions as long as the number of received bits is sufficiently long. The measurement is then repeated with the laser pulse present according to the timing diagram of Figure 72. If the number of bit errors increases in the presence of the laser strike on the frequency synthesizer, then a method for determining digital BER based on strikes of an analog block will have been demonstrated. Successful demonstration of this phenomena will allow a full scale experiment in a broad-beam environment to be conducted, which is necessary to collect statistics on random strikes at a given LET to determine cross-section.

The hypothesized mechanism that causes bit errors to occur based on transients at the frequency synthesizer output is rather straight forward. Digital modulation schemes use a number of different schemes to transmit data over a link. Two of the most popular for space-based applications for their robust performance are binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK). BPSK uses a single channel to map bits to predetermined phase states, while QPSK uses a similar technique but with two orthogonally-linked channels to double the number of bits transmitted per symbol. A radiation-induced transient on a frequency synthesizer will disturb the phase of the output signal, which acts as the LO for the down-conversion process in the receiver. This phase instability will impact the phase of the baseband signal, which expects a stable LO frequency. If the baseband phase disturbance has sufficient magnitude after filtering at the sampling instant to force the signal beyond the decision boundary, the receiver will incorrectly interpret the



(a) Large Transient With No Error

(b) Large Transient with Error

Figure 73: An illustration of how transient disturbances translate to bit errors.

phase modulation and produce an erroneous bit in that time slot. Such a scenario would seem increasingly likely as E_b/N_0 degrades.

An exaggerated phase transient that illustrates this concept is shown in Figure 73 for two values of E_b/N_0 in a QPSK modulation scheme. The large circles denote the 3σ boundaries of the Gaussian-distributed symbol constellation with no radiation-induced transients present. Assume transients in both figures produce a similar disturbance in the baseband signal, meaning the transient error vector (TEV) from the original sampled point to the disturbed sampled point is the same. Since the low SNR condition in Figure 73b places the original signal closer to the decision boundary, this TEV produces a bit error. The higher SNR condition in Figure 73a ensures that the original point is far enough away from the decision boundary that even a large transient will not produce a bit error. Note that with the large variation in constellation points under low SNR conditions it is possible for the original point to be far from the decision boundary so that a TEV causes no error as shown in the upper-left quadrant of Figure 73b. This implies that it is not necessary for every transient to

cause an error, and that TEV magnitude is not the sole determining factor. Instead, the prediction of an error will rely on the sum of the TEV and the traditional error vector (EV) from the ideal constellation. However, under the current experiment, there is no method to distinguish the TEV from the undisturbed EV. Measurements will always contain the sum of the two vectors. Therefore, we rely on the detection of increased errors under laser excitation as a proof of concept that synthesizer transients cause bit errors. However, this comes with the caveat that a negative result does not necessarily disprove the theory, particularly with only a single laser strike during the capture period. The "proof" thus lacks rigor, but can provide excellent insight toward further development.

The LMX2541 frequency synthesizer used as a DUT in this experiment was not intended for space applications, and therefore suffered from latch-up when the internal core digital circuitry was struck with a laser pulse. Three types of SEE were observed for this part. Latch-up between the rails was observed by hitting current compliance on the synthesizer power supply, requiring a power cycle in order to return to proper operation. A second effect was observed on strikes of digital bias control that caused a permanent jump in bias current but not all the way to current compliance. This part makes extensive use of digital to analog converters to adjust bias points and provide a degree of dynamic healing for process variations. We suspect that the effect observed here is latch-up occurring on a pass-gate switch, which is only capable of pulling a finite amount of current below the compliance threshold. Cycling power also restores normal bias levels, although functionality of the synthesizer was not noticeably disturbed. The third type of effect observed were the desired transient responses at the synthesizer output. These were found by looking for disturbances in the analog lock-detect output on an oscilloscope.

The theory was tested at an E_b/N_0 ratio of 8 dB for a BPSK transmission. The bits were transmitted at a data rate of 6 Mbps, with a total of 40 kbits received. Given the

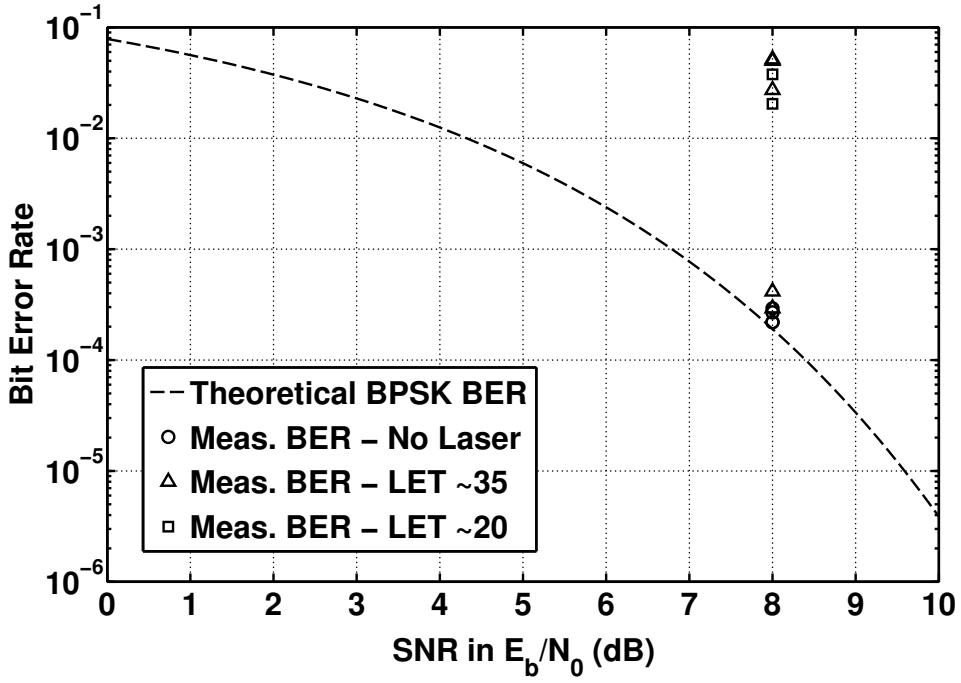


Figure 74: Bit error rate measurements show significant degradation under a laser pulse. The results do not seem to be strongly tied to the equivalent LET of the pulse.

slow processing capabilities of the HP89410A, each measurement took several minutes to process even though the data was captured in a few milliseconds. A sensitive area on the VCO circuit was found using the analog lock detect. The location selection was not particularly important for this experiment, but was one of several found around the die that produced fluctuations on the lock detect output. Several trials were conducted in this location to confirm the consistency of the results. The results shown in Figure 74 identify significant BER degradation attributed to laser strikes. With no laser present during data capture, the BER measurement is fairly consistent, producing between 9 and 12 errors out of the 40,960 bits captured. When the laser pulse is present, the error measurement can either produce errors nearly two orders of magnitude greater than the control case, or the errors can be in the same range. Adjusting the equivalent LET of the laser pulses did not change this result.

Based on the short pulse length of the laser and the response time of the loop to correct errors, only a small number of additional errors were expected compared to

the control case. The large number of errors generated are therefore very surprising, and indicate that closed-loop dynamic response is contributing to many of these errors rather than suppressing them. There are two possible explanations for the laser test runs that produced errors on the same order as the control tests with no laser present. The first possibility is the description shown in Figure 73b, where the sum of the transient error vector with the noise error vector produces a result that does not significantly disturb the constellation trajectory. However, with measurements indicating that more than a single symbol is affected during a radiation-induced transient, this conclusion cannot be verified from this data. An alternative explanation might be that the laser pulse did not induce a transient at all during that particular strike. A new measurement that captures the lock detect waveform on the oscilloscope at the same time as the BER data capture is needed to conclusively determine the observed effect.

Although more errors are clearly produced when the laser pulse is present, the BER plot of Figure 74 gives no indication as to where those errors occur relative to the laser pulse. This visualization can be seen in Figure 75. The captured symbols are shown on the x-axis in the order they are captured. At the 6 Mbps data rate, each symbol therefore represents about 167 ns of time. Symbols that are correct have a white background, while symbols that are in error are represented by a black line. The result is a bar code-style plot that can identify groupings of errors in the time-domain. With no laser present, errors are sporadic and each error can be counted as an individual line on the plot. With the laser present, however, large black regions on the plot represent big chunks of data that are in error. The red dashed line in Figure 75 shows the calculated location of the laser strike. Although this calculation is a coarse estimate based on the resolution of the pulse generator available, several measurements seem to indicate some time elapses between the laser incidence and the first large block of data errors. Large chunks of data errors also seem to come in

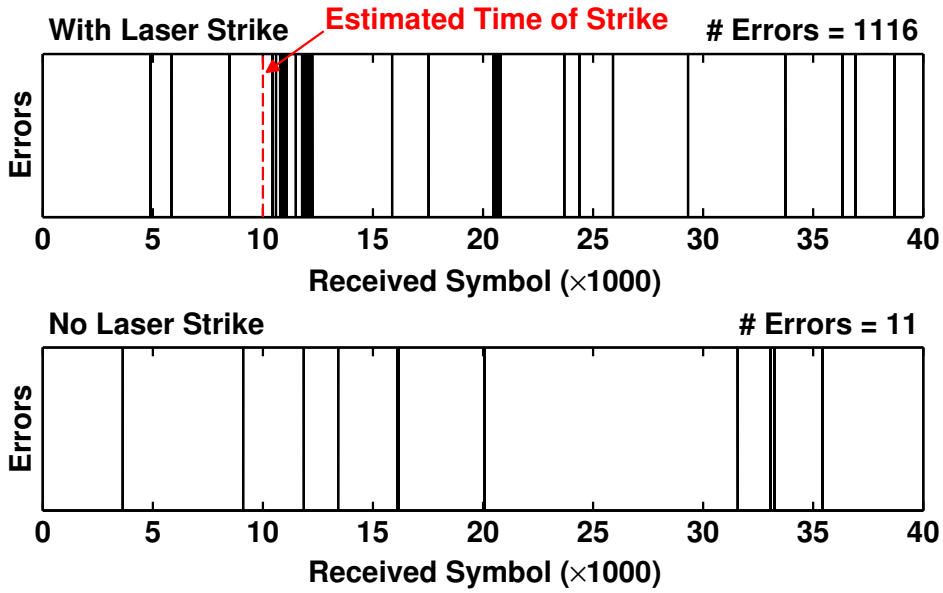


Figure 75: Time-domain "bar code" visualization of symbol errors. White space indicates a correct symbol, while a black line indicates a symbol error. The thick black bars near the estimated laser strike clearly indicate that the errors are laser-induced.

bands that are thicker and more frequent near the laser strike and fade away as capture time progresses, which also seems indicative of closed-loop dynamics attempting to re-establish a locked condition on the frequency synthesizer.

There are many improvements that can be made to the measurement setup in future experiments. Most of these improvements would reduce the measurement time and increase the reliability of the measurement. Processing the raw capture buffer on a laptop rather than the HP89410 would allow faster processing of results a more customizable control over channel synchronization than the first round results allowed. However, these initial measurements clearly show that radiation-induced transients can have a significant impact on communication bit errors. Further effort is needed to identify the closed-loop characteristics that exacerbate these errors as well as develop a full BER curve across E_b/N_0. That curve can then be used to test simulations based upon the ideas developed here to explain the expected bit errors under arbitrary

conditions. With the development of a latch-up immune frequency synthesizer, these theories can be put to the ultimate test in a broad-beam environment where statistical bit error predictions for random strikes across the entire die can be tested.

CHAPTER V

SUMMARY

This dissertation has focused on the application of SiGe technology to problems involving frequency synthesis. Despite the broad range of topics covered under this umbrella, all share a common underlying process. Whether the measurement is residual phase noise or bit error rate, each experiment outlined in this document has relied on a relatively exotic measurement technique to achieve a deeper understanding of the synthesizer and its related circuit blocks than was previously known. The results of these studies have resulted in a number of contributions to the community at large.

The phase noise measurement system developed and built for this research provides our group with unparalleled ability to measure phase noise in any form. Although most of the measurement techniques were developed over thirty years ago, this system can still claim to have excellent performance per unit cost compared to other commercial offerings from vendors such as Agilent, Wenzel, Aeroflex, and Holzworth. In its final form, the system can measure carrier frequencies up to 18 GHz and offset frequencies to 10 MHz at a cost estimated at $40K. The 10 MHz bandwidth sets this system apart from most others and is enabled in large part by the recent introduction of the LMH6629 SiGe op-amp. The documentation provided in Chapter 2 is also one of the most inclusive references for phase noise measurement theory published recently. For example, although the FM calibration routine is known to have existed prior to this research, this document is the first known place to lay down the exact theory of operation in open literature. It is hoped that this system will provide the SiGe research group with a tool to probe the limits of the SiGe HBT for years to come.

The availability of the phase noise measurement system has enabled a number of contributions that would have been otherwise impossible. The impact of current gain, β, on phase noise was identified through comparisons of matched performance complementary HBTs. Many of the cross-check measurements used to eliminate alternative interpretations relied on the knowledge of the slope and corner frequencies of the phase noise plot at close-in frequencies, which would not have been possible using a spectrum analyzer alone. Residual phase noise measurements confirmed the improvement of the novel latch technique, and helped to demonstrate best-in-class phase noise performance for the frequency dividers. These measurements would not have been possible without the phase noise measurement system. Finally, the unique capabilities of this system were leveraged to devise a new method for measuring AM/PM distortion in HBTs. This technique gives unique insight into device linearity and applications for these measurements are ripe for development.

Understanding the impact of radiation effects on frequency synthesizers is a nascent field of study gaining increasing importance. The work presented here has made significant strides in improving the understanding of several of the unique phenomena at play in these systems. First, a theory describing the mechanisms behind SET phenomena in resonant tank oscillators has been presented and confirmed with measurements. This theory provides critical understanding to go beyond the empirical observations presented in previous literature for resonant tank circuits. An investigation of mitigation techniques in charge pumps is the first in depth analysis of this critically sensitive circuit block. An investigation of proven digital mitigation techniques in shift registers applied to frequency dividers has revealed a different mechanism at work for these circuits that renders the techniques ineffective. When a complete theory of the closed-loop transient response was published for the frequency synthesizer in [62], this work built upon that theory to produce steps toward translating SET information into BER metrics meaningful to a system designer. Preliminary

results from a new measurement technique designed to demonstrate this translation have been the first to prove this new concept.

5.1 Remaining Problems

This research pursued many different circuit approaches and applications where SiGe technology might have a positive impact on frequency synthesizer performance. Some of those efforts produced results that revealed additional interesting problems worthy of further investigation, while others did not. My intentions moving forward are to focus on the problems involving radiation studies outlined in Section 5.1.2. The problems associated with radiation tolerance tend to have more depth and a greater potential impact than the still interesting but less cohesive problems identified through advanced phase noise measurements. However, all of the identified problems are listed here in the interest of completeness.

5.1.1 Phase Noise Measurements

The phase noise measurement system built for this research provides a more cost effective and flexible platform for measurements than any commercially available product. As such, there are a wide variety of measurement possibilities that remain unexplored. Some of the most intriguing possibilities here lie in the exploration injection-locking phenomena in oscillators. Such work would likely expand upon the setup outlined in [79], although no specific experiments have been identified at this time.

The study of phase noise in matched-performance complementary SiGe HBTs leads directly to interesting further studies of SiGe HBT device physics applied specifically to autonomous circuits. The results of the study hypothesized that the observed difference in phase noise between a high-speed vertical *pnp* HBT and an identical circuit using a matched-performance *npn* HBT could be attributed to the difference in DC current gain, β. Further exploration of this hypothesis would likely begin with the

development of advanced mixed-mode simulations in TCAD that could combine the dynamic circuit simulation capabilities of the Cadence Suite with rigorous solutions of the three-dimensional device model. Such simulations would present the best indications of the validity of the effect short of physically building the devices. If these simulation results show promise, a much more effective case for the more expensive prototype fabrication could be made.

This research has outlined a unique method for characterizing the AM/PM distortion in individual transistors. However, demonstration of how these measurements might be utilized to produce oscillators with superior phase noise has yet to be carried out. In order for the developed measurement techniques to be useful, a procedural design implementation should be clearly defined. This procedure would follow a microwave-style graphical approach to oscillator design similar to the technique developed by Kurokawa [50]. Modifications to Kurokawa's technique would involve separate implementation of the AM/PM noise terms that are now directly measured values.

5.1.2 Radiation Studies

Exploration of single-event radiation effects on wireless communications front-ends is a field with extensive possibilities for future research because it remains relatively unexplored. One of the primary reasons for this lack of developed theory stems from a lack of measurement techniques and critical metrics to characterize the analog nature of these circuit transients. This dissertation has made a significant effort to push this characterization forward for circuits involved with frequency synthesis. While significant progress has been made in this regard, a considerable amount of work remains to produce a well-defined design procedure that will be useful for system designers with defined bit error rate specifications.

The primary goal of this research is to have a procedure that translates the random charge injected into a circuit during a heavy ion strike into an accurate statistical prediction of bit errors. The first steps taken here have been to characterize metrics and mitigation strategies for individual circuit blocks of a frequency synthesizer PLL. A complete theory for closed-loop PLL transients was subsequently published, furthering our understanding of potential phenomena [62]. Our response has been to utilize this theory toward a framework translating transient waveforms into BER predictions. However, the linear model developed in [62] is likely not the only model that will be necessary. Most IC implementations of PLLs are mixed signal circuits that fundamentally incorporate sampled, discrete signals. The approximations that allow simplification to a linearized model will only hold over a narrow range of conditions as outlined in [14]. Understanding transient impact at these fringes is a topic worthy of consideration going forward.

The theory developed here for understanding transients in oscillators has provided a technique for statistically predicting the transient response of a time-variant circuit. However, the severe collapse-style transients observed during measurements have not been sufficiently characterized. A working hypothesis has been provided offering an explanation for the underlying mechanism, but this has never been directly tested. Furthermore, the direct measurement method used to characterize the transient signals is difficult for high frequency signals. Rather than using an oscilloscope directly, a better solution might be to use a phase measurement setup similar to the phase noise system back-end in parallel with an envelope tracking circuit. Thus, the envelope tracking could provide magnitude information, while the mixer phase detector provides angle information. Vector measurements of the transients would then be possible and the characterization metrics would be easier to analyze.

Finally, improvement of the BER measurement system described in Section 4.5 is possible. During first pass testing, the setup used could capture nearly 500,000

symbols of data in a single capture window, but processing that data took nearly a half hour given the relatively old computing power of the HP89410A. Future plans for the measurement system involve offloading the processing requirements to the laptop, which can perform much faster, as well as modifying the downconverter circuitry to enable measurement of the LO and the baseband output at the same time. The measured data shown in Section 4.5 is also only preliminary data that proves the concept of translating ion-induced transients to bit errors. The test was conducted on a laser system where strikes could be localized for cost-reduction purposes. A final proof will need to come in the form of a broadbeam experiment where ions strike the part randomly and meaningful statistics can be gathered. Conducting this test also means that the part must be immune to latch-up events caused by ion strikes, a condition not currently met by nearly all of the commercially available synthesizer products.

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